ANALYSIS AND DESIGN OF LCC-TYPE ZERO VOLTAGE SWITCHING RESONANT CONVERTER USING STATE-PLANE DIAGRAM

BY

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A THESIS SUBMITTED IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR
THE DEGREE OF MASTER OF ENGINEERING IN
ELECTRICAL AND COMPUTER ENGINEERING
COLLEGE OF ENGINEERING

GRADUATE SCHOOL, RANGSIT UNIVERSITY
ACADEMIC YEAR 2022

Thesis entitled

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was submitted in partial fulfillment of the requirements

for the degree of Master of Engineering in Electrical and Computer Engineering

Rangsit University

Academic Year 2022

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February 20, 2023

Acknowledgements

I would like to many thanks sincerely with my both instructors, Asst. Prof. Somboon Sooksatra, Ph.D. and Asst. Prof. Wanchai Subsingha, Ph.D. for their advices and giving much knowledge. Also, I would like to many thanks sincerely to Miss Wanchanok Ratsamee for giving power electrical notes (no. 1-8), her homework and many advices as my colleague.

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Thesis Title : Analysis and Design of LCC-Type Zero Voltage Switching Resonant Converter Using State-Plane Diagram

Program : Master of Engineering in Electrical and Computer Engineering

Thesis Advisor : Asst. Prof. Somboon Sooksatra, Ph.D.

Abstract

In this thesis, steady state analysis and design of LCC-type zero voltage switching resonant converter using state-plane diagram are presented. The converter proposed is separated into three parts for analysis, that are source circuit, resonant tank circuit and load circuit. There exist equivalent circuits of ten sequential modes for this converter. The state-plane diagram is presented from analyzing all equivalent circuits of ten sequential modes. Each sequential mode will be derived to get the normalized inductor current and capacitor voltage in functions of time domain. The waveforms of these normalized current and voltage versus time of all sequential modes are simulated from OCTAVE program. The normalized output voltage or converter gain calculated versus normalized switching frequency for each load current condition is shown. Finally, the simulated circuit of the proposed converter is generated to confirm the analysis of converter using state-plane diagram approach.

(Total 95 pages)

Keywords: State-plane diagram, zero voltage switching, resonant converter, asymmetrical converter

Student's Signature …..... Thesis Advisor's Signature .....

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Chapter 1

Introduction

1.1 Power Converter

Power Electronics (PE) is used to convert characteristic of power from source to output or load.

The power converter is mainly classified to four types according to type of input and output current as shown in figure 1.1.

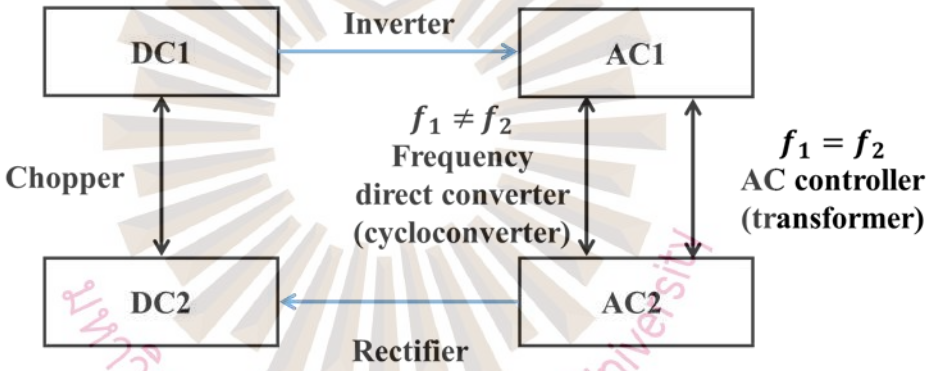


Figure 1.1 Power converter specification
Source: Sunpower Electronics, 2022

1.1.1 The AC to DC converter is normally called the rectifier. It can be categorized in detail as

1) Uncontrollable Rectifier

1.1) Single-phase half-bridge

1.1.1) Resistive output circuit (R)

1.1.2) Capacitive output circuit (RC)

1.1.3) Inductive output circuit (LR)

1.1.4) Inductive output circuit with capacitor (LCR)

1.2) Single-phase full-bridge

1.3) Three-phase half-bridge

1.4) Three-phase full-bridge

2) controllable Rectifier

2.1) Full-Bridge

2.2) Half-bridge

The classification of a rectifier can be shown in Figure 1.1.

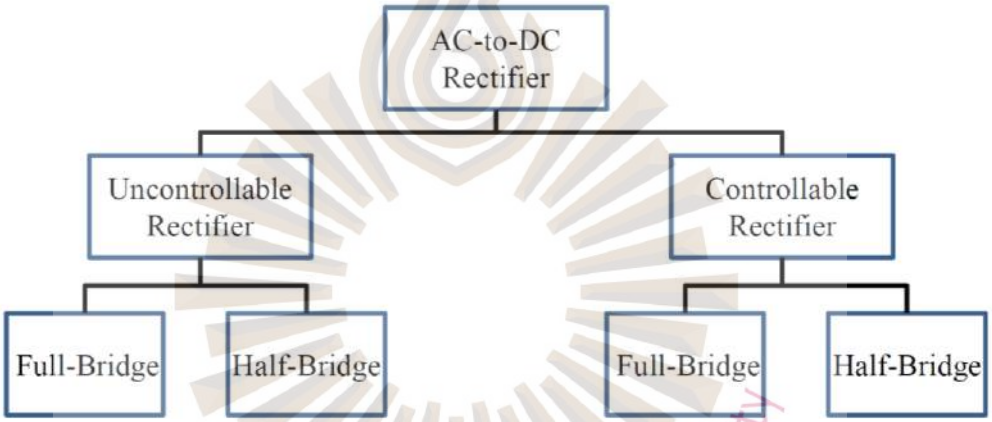


Figure 1.2 The classification of a rectifier

Source: Sooksatra, 2021

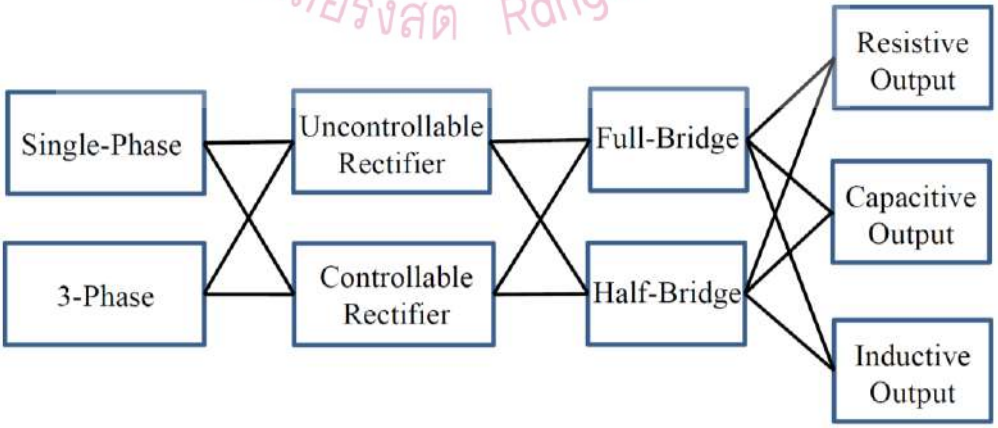


Figure 1.3 Possibilities of Rectifier Circuits

Source: Sooksatra, 2021

1.1.2 The AC to AC can be categorized as

1) AC voltage controller

2) AC voltage stabilizer

3) Frequency converter

4) Power factor converter

1.1.3 The DC to DC is called voltage or current converter can be categorized to

1) Buck converter

2) Boost converter

3) Buck-Boost converter

4) Ground separation system converter

1.1.4 The DC to AC is normally called Inverter circuit. It can be categorized according to operating topology.

1) Half bridge topology inverter

2) Full bridge topology inverter

3) Push-Pull topology inverter

1.2 The DC to DC converter

There are three basic DC to DC converter normally used that are buck converter, boost converter, buck-boost converter.

1.2.1 Buck converter is used to step-down output voltage that is shown in Figure 1.4

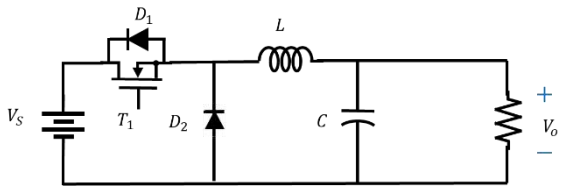


Figure 1.4 Buck converter

Source: Sunpower Electronics, 2022

1.2.2 Boost converter is used to step-up output voltage that is shown in Figure 1.5

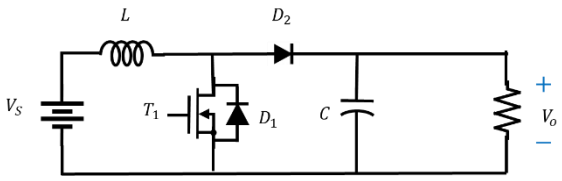


Figure 1.5 Boost converter

Source: Sunpower Electronics, 2022

1.2.3 Buck-boost converter is used to step-up or step-down output voltage as a condition previously determined that is shown in Figure 1.6

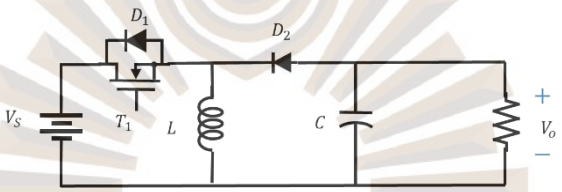


Figure 1.6 Buck-boost converter

Source: Sunpower Electronics, 2022

1.3 Resonant converter

A resonant converter is a converter that comprise of source circuit, resonant tank circuit and load circuit. The important part of a resonant converter is resonant tank circuit that must be composed of inductor (L) and capacitor (C). The resonant tank circuit operates as energy transfer from source circuit to load circuit.

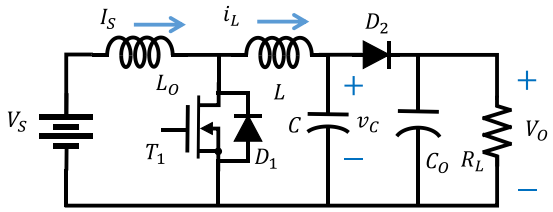


Figure 1.7 Example of resonant converter circuit

Source: Sooksatra & Subsingha, 2020

From Figure 1.7, In order to analyze a circuit easily. The circuit must be simplified to Figure 1.8 according to the concept in A Unified approach to the classification and analyses of resonant converters.

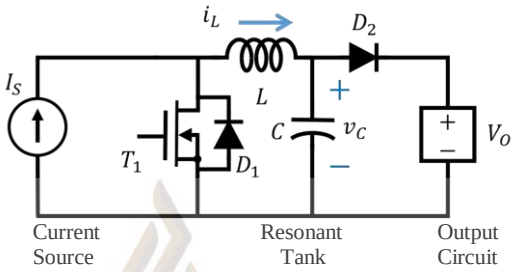


Figure 1.8 Equivalent circuit of the converter with current source and voltage sink as source and output circuits, respectively

Source: Sooksatra & Subsingha, 2020

1.4 Research motivation

From the paper of Performance characteristic of the full bridge zero voltage switching PWM resonant converter, a researcher of this thesis wants to analyze and design zero voltage switching resonant converter (ZVS) that produces the same output with this paper but use less amount of MOSFETs in a converter to reduce a size and weight of a converter.

Chapter 2

Literature Review

2.1 Literature review of ZCS Boost Converter with Inductive Output Filter.

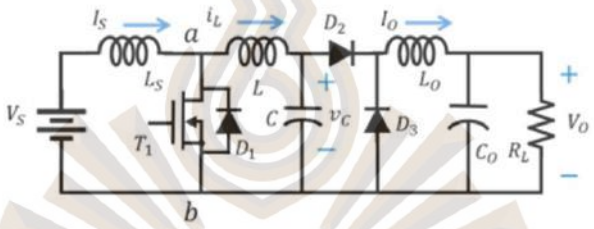


Figure 2.1 The circuit of ZCS Boost Converter with Inductive Output Filter
Source: Sooksatra & Subsingha, 2020

2.1.1 Research Objective

The researches want to design the ZCS boost converter with inductive output filter by using state-plane diagram approach. From $P = iv$, many researches try to diminish voltage (v) to zero which is also reducing power loss to zero but this research try to diminish current (i) to zero. a researcher wants to reduce power switching loss due to new equipment need more high power to operate. High frequency makes equipment to be smaller size but high frequency still make more power loss.

2.1.2 Research methodology

The researchers separate to analyze a circuit into three parts that are source, resonant tank, load circuit as shown in Figure 2.2. Then a circuit must be simplified to circuit simplification to analyze easily. Then a researcher uses state-plane diagram approach to analyze a circuit to get diagram of v_{nC} in x-axis and i_{nL} in y-axis. Then the

researchers normalize all variable to get equation of normalized capacitor voltage (v_{nC}) and the normalized inductor current (i_{nL}) in time domain for each sequential mode. After that they plotted waveform of i_{nL} and v_{nC} versus time in OCTAVE (MATLAB open source compatible). Finally, a circuit was generated to simulate the normalized inductor current (i_{nL}) and normalized capacitor voltage (v_{nC}) in time domain for confirming the wave form from state-plane diagram approach.

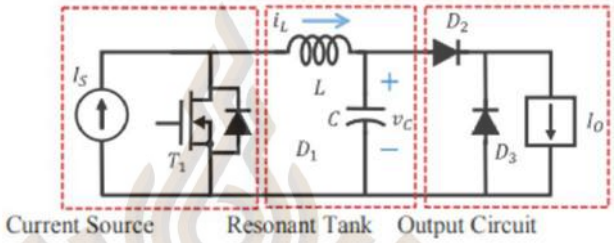


Figure 2.2 The equivalent circuit of ZCS Boost Converter with Inductive Output Filter

Source: Sooksatra & Subsingha, 2020

2.1.2.1 Representation of State-plane Diagram

There are five sequential modes from this proposed topology. Each of sequential mode has own equation that represent characteristic of itself.

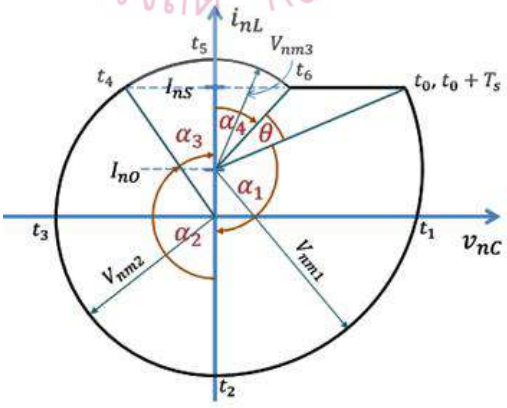


Figure 2.3 State-plane diagram of ZCS Boost Converter with Inductive Output Filter

Source: Sooksatra & Subsingha, 2020

The variables calculated to get state-plane diagram approach must be normalized. State-plane diagram composes of normalized capacitor voltage (v_{nC}) being x-axis versus the normalized inductor current (i_{nL}) being y-axis.

Wave form of the normalized inductor current (i_{nL}) and normalized capacitor voltage (v_{nC}) plotted by OCTAVE (MATLAB open source compatible) in time domain in Figure 2.4

A circuit was generated to simulate the normalized inductor current (i_{nL}) and normalized capacitor voltage (v_{nC}) in time domain for confirming the wave form from state-plane diagram approach.

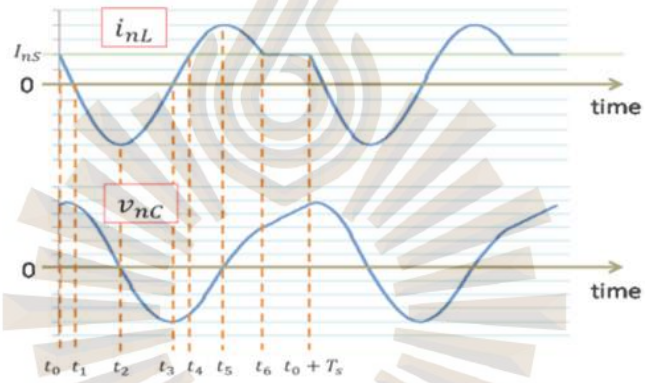


Figure 2.4 Waveforms of i_{nL} and v_{nC} derived from the state-plane diagram

Source: Sooksatra & Subsingha, 2020

2.1.3 Conclusion

A state-plane diagram approach can be used to analyze the proposed resonant converter accurately and easy to understand.

Furthermore, a circuit must be second order circuit converter. A higher order circuit converter cannot be analyzed by state-plane diagram approach.

2.2 Literature review of Light Load Efficiency Enhancement of the LLC Resonant Converter

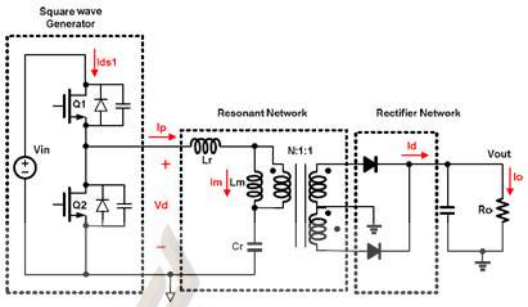


Figure 2.5 Schematic of half bridge LLC resonant converter

Source: Qin, Moussaoui, Liu & Miller 2011

2.2.1 Research Objective

$$f_r = 2\pi \frac{1}{\sqrt{L_r C_r}} \quad (2\text{-}1)$$

$$Z_O = \sqrt{\frac{L_r}{C_r}} \quad (2\text{-}2)$$

$$Q = \frac{Z_O}{R_{ac}} \quad (2\text{-}3)$$

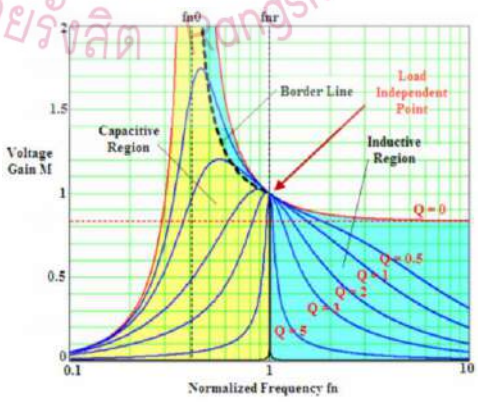


Figure 2.6 Control characteristic of traditional LLC converter

Source: Qin, Moussaoui, Liu & Miller 2011

LLC converter operates in inductive region. When Z_O is decreasing from equation 2.3, it will make Q decrease. From Figure 2.6, in order to generate the same voltage gain (M), a converter must operate in higher normalized frequency (f_n). A converter sometimes can not operate in high frequency due to a limitation of the controller IC, so the researchers proposed ZVS LLC resonant converter to improve efficiency from traditional converter in light load condition.

2.2.2 Research methodology

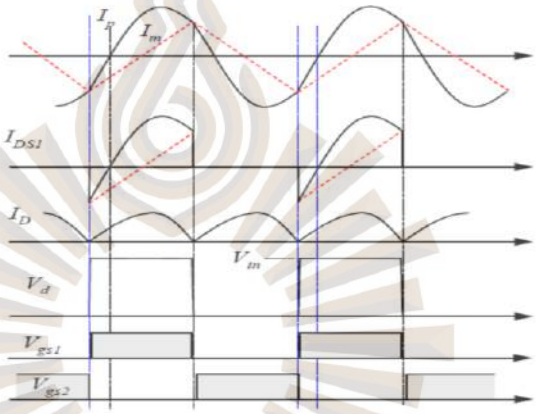


Figure 2.7 Typical waveforms of LLC resonant converter

Source: Qin, Moussaoui, Liu & Miller 2011

From Figure 2.7, Because the current I_p of resonant network is not coincident with the voltage $V_g(Q2)$ of MOSFET, it will make the MOSFETs operate with zero voltage switching.

Researchers created control circuit for generating gate drive signal of MOSFETs Q_1 and Q_2.

In order to confirm the proposed approach, the circuit of proposed approach was built and connected to evaluation board. The simulation result wave forms of both light load and heavy load condition were generated

Most applications require high power (high voltage gain) and smaller size of passive components. From equation 2.1, higher value of f_r makes L_r and C_r lowering. so increasing switching frequency can make passive components smaller. However,

increasing switching frequency will make the converter have lower voltage gain (M) on the same Q (from Figure 2.6).

On high normalized frequency range from Figure 2.6, a converter gives low voltage gain.

2.2.3 Conclusion

The researchers show a graph of efficiency versus load. It shows that an efficiency of a light load condition in proposed hysteretic is better than in conventional variable frequency control. The researcher improves the efficiency of light load, whereas conventional variable frequency control can not make high efficiency in light load condition.

2.3 Literature review of ZVS Analysis of Asymmetrical Half-Bridge Converter

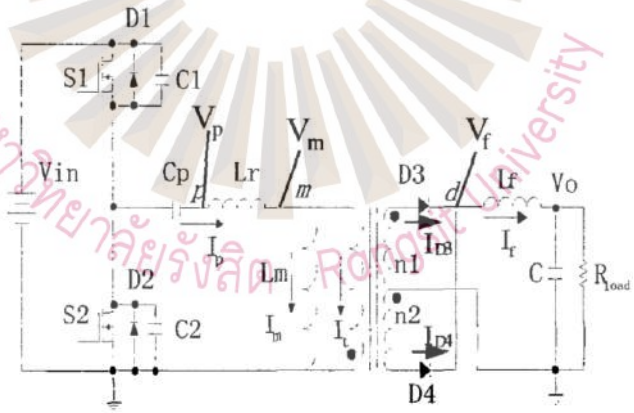


Figure 2.8 Asymmetrical half-bridge topology

Source: Hsieh & Kuo 2005

2.3.1 Research Objective

The researcher intended to design high power converter output, so the converter circuit could have very high frequency. Zero voltage switching makes a converter minimize power losses due to the switching loss on many loads.

2.3.2 Research methodology

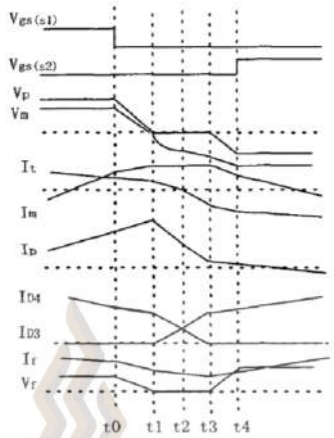


Figure 2.9 The transition process of ZVS

Source: Hsieh & Kuo 2005

The researchers tried to make switches be operated with zero-voltage switching. A circuit is resonant by using leakage inductance of a transformer and parasitic capacitance. MOSFETs switching operation under zero voltage of parasite capacitor will make ZVS resonant circuit. The MOSFET turned on when D-S junction of MOSFET is zero voltage as described in detail of time interval.

2.3.3 Conclusion

A new gate drive signal is presented and applied in a buck ZVS-QRC. This paper present ZVS technique for high frequency operation for increasing output efficiency. However, the researcher still recommends future interesting operation of developing converter.

1) Dissipation of voltage over the MOSFET during switching will make a converter give higher output due to lossless operation.

2) Increasing output range of operation with zero voltage operation of MOSFET.

Table 2.1 Literature review of ZCS Boost Converter with Inductive Output Filter

Title	ZCS Boost Converter with Inductive output Filter
Objective	• In order to design the ZCS boost converter to give more efficiency by using state-plane diagram approach • a researcher wants to reduce power switching loss due to new equipment need more high power to operate. However, high frequency make equipment to be smaller size but high frequency still make more power loss.
Research Methodology	• The proposed circuit is separated into three parts, that are source circuit, resonant tank circuit and load circuit for analysis. • Then a researcher uses state-plane diagram approach to analyze a circuit. • the researchers normalize all variable to get equation of normalized capacitor voltage (v_{nC}) and the normalized inductor current (i_{nL}) in time domain for each sequential mode. After that they plotted wave form of i_{nL} and v_{nC} versus time in OCTAVE (MATLAB open source compatible).
Result of Research	• The researcher can design the ZCS_IF boost converter by turn-on MOSFET on the time that current of i_{nl} is not change from previous value • Precise calculation for a second order resonant circuit can be achieved by using state-plane diagram approach.
Conclusion and Future Application	• A state-plane diagram approach can be used for analysis with other resonant converters accurately in second order only. • Using State-Plane Diagram approach makes the converter easy to be analyzed and understood. • Furthermore, a circuit must be second order circuit converter. A higher order circuit converter cannot be analyzed by state-plane diagram approach.

Table 2.1 Literature review of ZCS Boost Converter with Inductive Output Filter (continued)

Analogy and relation to my work	• This paper uses the same research methodology with this thesis, that is state-plane diagram approach. • There is another way of diminishing loss, these researchers try to reduce switching loss of current (ZCS) in resonant converter but this thesis try to reduce switching loss of voltage (ZVS) in resonant converter. • There are all normalized parameters the same as my work.

Table 2.2 Literature review of Light Load Efficiency Enhancement of the LLC Resonant Converter

Title	Light Load Efficiency Enhancement of a LLC Resonant Converter
Objective	• The researchers want to create ZVS LLC resonant converter to improve efficiency from traditional converter in light load condition.
Research Methodology	• Because The current I_p of resonant network is not coincident with the voltage $V_g(Q2)$ of MOSFET, it will make the MOSFETs operate with zero voltage switching. • Researchers create control circuit for generating gate drive signal of MOSFETs Q_1 and Q_2. • In order to confirm the proposed approach, the circuit of proposed approach was built and connected to evaluation board. The simulation result wave forms of both light load and heavy load condition were generated.
Result of Research	• The researcher improves the efficiency of light load, whereas conventional variable frequency control can not make high efficiency in light load condition. • The researchers show the result waveforms both light load (I=0.1 A) and heavy load (I=1 A) that conform with proposed hysteretic control scheme.
Conclusion and Future Application	• The researchers show a graph of efficiency versus load. It shows that an efficiency of a light load condition in proposed hysteretic is better than in conventional variable frequency control. • The researcher improves the efficiency of light load, whereas conventional variable frequency control can not make high efficiency in light load condition.
Analogy and relation to my work	• A researcher tries to reduce switching loss by making current not coincident with voltage to the resonant tank so the LLC resonant converter will operate by zero voltage switching. Additionally, the researcher also improves the light load efficiency.

Table 2.3 Literature review of Literature review of ZVS Analysis of Asymmetrical Half-Bridge Converter

Title	ZVS Analysis of Asymmetrical Half-Bridge Converter
Objective	• The researchers want to create ZVS LLC resonant converter to improve efficiency from traditional converter in light load condition.
Research Methodology	• The researchers want to make zero-voltage switching in this circuit. • A circuit is resonant by using leakage inductance of a transformer and parasit capacitance • MOSFET Switching operation under zero voltage of parasite capacitor will make ZVS resonant circuit. • The researcher will turn on MOSFET when both gate drive signal of MOSFETs are zero voltage as described in detail of time interval. • Researchers create a circuit to confirm an analysis of a converter.
Result of Research	• This paper present ZVS technique for very high frequency operation for increasing output. • In the case of light load, the converter efficiency reduced due to non zero voltage switching. • A paper present high efficiency of a circuit from a graph of load current versus efficiency. • A result wave form will show turning on of both MOSFETs on zero voltage switching.
Conclusion and Future Application	• A new gate drive signal is presented and applied in a buck ZVS-QRC. This paper present ZVS technique for high frequency operation for increasing output efficiency. • However, the researcher still recommends future interesting operation of developing converter.

Table 2.3 Literature review of Literature review of ZVS Analysis of Asymmetrical Half-Bridge Converter (continued)

Conclusion and Future Application	1. Dissipation of voltage over the MOSFET during switching will make a converter give higher output due to lossless operation. 2. Increasing output range of operation with zero voltage operation of MOSFET.
Analogy and relation to my work	• The researchers try to make zero voltage switching of MOSFET in quasi-resonant converter. The circuit is made to give high efficiency with high frequency and only heavy load. • This circuit use MOSFET with parallel diode as bidirectional device and parasite capacitor as a component for resonant circuit. • This circuit consisted of output inductor that is assumed to be relatively large to maintain approximately constant current. • A load circuit of the converter is the same as the converter of this thesis. • There is high value of a filter inductance that is the same as circuit in this thesis. • A circuit is asymmetrical haft bridge switch of quasi resonant converter that is the same as this thesis. • Because asymmetrical switch will make a source circuit of a converter have three result according to principle of two MOSFETs connected with voltage source.

Chapter 3

Research Methodology

3.1General Concept

Steady state condition is a stable condition of a circuit after transient condition has passed.

Steady state condition as a very necessary part because many design processes of electronic circuit are in a part of steady state condition.

Transient condition has a very short time period after a circuit is energized by electrical power and followed by steady state condition. The transient condition is classified to three types of damping that are underdamping, overdamping and critical damping.

During steady state,

1) Every current and current wave forms must be periodic. Hence, for any of time during steady state, where donates for any signal of current and voltage in the circuit.

$$x(t) = x(t + T_s) \tag{3-1}$$

where x denotes for any signal of current and voltage in the circuit.

2) The average voltage across an inductor over a switching period must be zero.

$$\frac{1}{T_s}\int_{t}^{t+T_s} v_L dt = 0 \tag{3-2}$$

Prove:

$$V_L = L\frac{di_L}{dt} \tag{3-3}$$

$$\int_{t}^{t+T_s} v_L dt = L[i_L(t + T_s) - i_L(t)] \tag{3-4}$$

Since i_L is periodic, the right side becomes zero, as well as the left side.

3) The average current through a capacitor over a switching period must be zero.

$$\frac{1}{T_s}\int_{t}^{t+T_s} i_C dt = 0 \tag{3-5}$$

Prove:

$$i_C = C\frac{dv_C}{dt} \tag{3-6}$$

$$\int_{t}^{t+T_s} i_C dt = C[v_C(t+T_s) - v_C(t)] \tag{3-7}$$

Since v_C is periodic, the right side becomes zero, and so the left side.

3.2 Converter analysis and design – Steady state analysis

The following conditions will be used for steady state analysis

1) All components are ideal and no loss.

2) Circuit simplification is utilized.

3) Energy transferred in current or voltage buffer and energy out during a switching period must be equal.

Steady state analysis procedure

1) Identify equations related to the conditions mentioned above.

2) Derived for relation of V_o and V_s in terms of control parameter, which is duty ratio (D) for this case.

3) Derive for component stress for other components in the circuit in terms of output voltage (V_o) or output current (I_o).

3.3 Circuit simplification

Besides switching devices and load, the main components used for PWM converter are inductor (L) and capacitor (C). In addition to storing energy, these two components are used for smoothing current and voltage, respectively. In most

applications, the PWM converters are used in CCM, so the current flowing through any and the voltage across any can be assumed to be constant.

In this case:

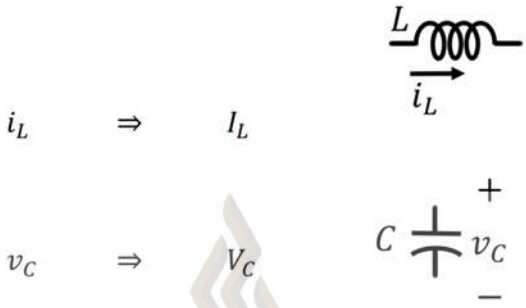


Figure 3.1 Symbols of constant inductor current and capacitor voltage

Source: Sooksatra, 2021

Inductor directly connected to voltage source: The circuit of an inductor directly connected to a voltage source as shown in Figure 3.2 can be treated as a dc current source (I_S) since the current through the inductor is assumed to be constant.

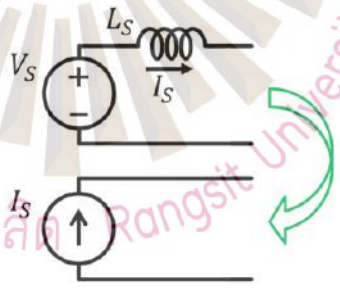


Figure 3.2 Circuit simplification of Inductor directly connected to voltage source

Source: Sooksatra, 2021

Inductor directly connected to load: The circuit of an inductor directly connected to load as shown in Figure 3.3 can be treated as a dc current sink (I_o) since the current through the inductor is assumed to be constant. The reason for being called current sink is that the circuit only consumes energy from any other component.

Note: The capacitor C_O in the circuit is functioned when there is a load change.

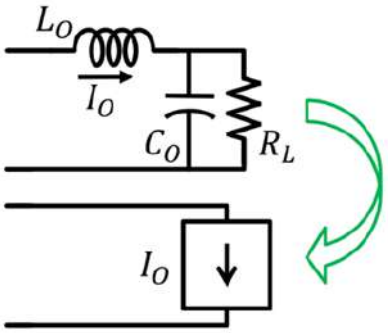


Figure 3.3 Circuit simplification of Inductor directly connected to load

Source: Sooksatra, 2021

Capacitor directly connected to load: The circuit of a capacitor directly connected to load as shown in Figure 3.4 can be treated as a dc voltage sink (V_o) since the voltage across the capacitor is assumed to be constant. The reason for being called voltage sink is that the circuit only consumes energy from any other component.

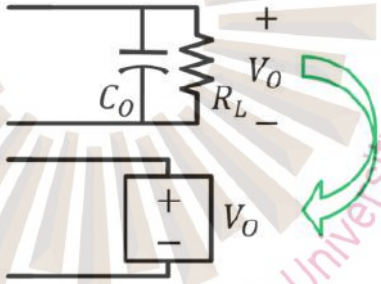


Figure 3.4 Circuit simplification of capacitor directly connected to load

Source: Sooksatra, 2021

Inductor and capacitor used as energy buffers: Some converter topologies have either inductor or capacitor used for receiving energy from source circuit and transferring to load circuit. In this document, these will be called “Current Buffer” and “Voltage Buffer”, respectively, and are represented, accordingly, by the symbols shown in Figure 3.5.

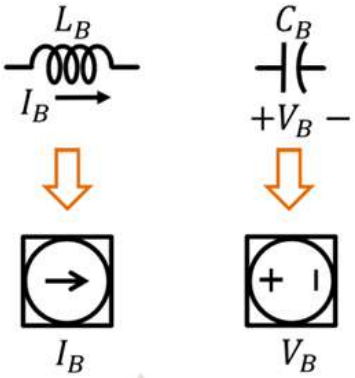


Figure 3.5 Symbols of Inductor and capacitor used as energy buffers

Source: Sooksatra, 2021

	Source	Sink	Buffer
Current	I_S	I_O	I_B
Voltage	V_S	V_O	V_B

Figure 3.6 List of components used in simplified circuits of conventional PWM converters

Source: Sooksatra, 2021

Rules for energy transfer:

1) Energy cannot be transferred from current type to current type.

2) Energy cannot be transferred from voltage type to voltage type.

3) Sources can only transfer energy out.

4) Sinks can only receive energy.

5) Buffers can transfer out and receive energy.

6) During a switching period in steady state, energy received by a buffer and energy transferred by the buffer must be the same amount.

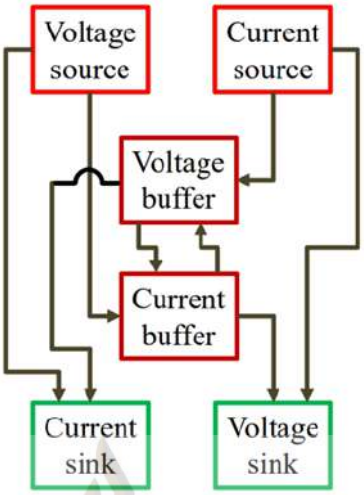


Figure 3.7 Possibilities of energy flow among all components in a converter

Source: Sooksatra, 2021

3.4 Classification of Resonant Converter

3.4.1 Purely resonant converter

Inductor current (i_L) and capacitor voltage (v_C) of LC resonant circuit change resonantly during the switching period.

3.4.2 Quasi resonant converter

Inductor current (i_L) and capacitor voltage (v_C) of LC resonant circuit have both resonant change and linear change during the switching period.

3.5 Modes of Operations

3.5.1 Continuous conduction mode (CCM)

Inductor current (i_L) continuously changes during a switching period. There is always current flow through inductor every switching period.

3.5.2 Discontinuous conduction mode (DCM)

There is at least one time interval with inductor current (i_L) being zero during a switching period. There is one or more of switching periods that no current (i_L) flows through an inductor (open circuit).

Time Domain Analysis of PWM Converter

Buck converter

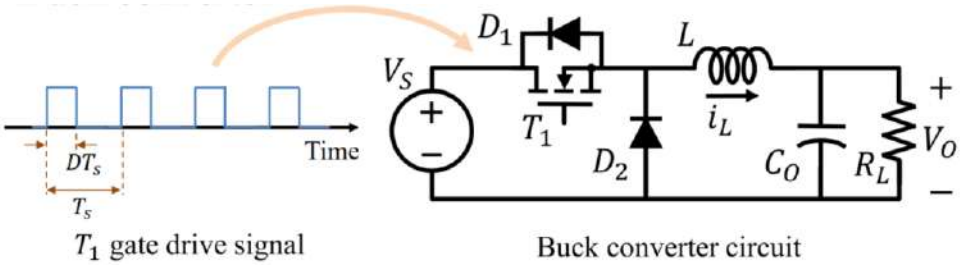


Figure 3.8 Operating gate drive signal for MOSFET T_1 of buck converter circuit

Source: Sooksatra, 2021

Assumption:

1) All devices are assumed to be ideal.

2) MOSFET is turned on and off periodically with period of T_s .

3) During a switching period, T_1 is turned on for DT_s, where is the duty ratio and $0 \leq D \leq 1$.

4) The capacitor is relatively large, so can be assumed constant.

Buck converter - Continuous conduction mode (CCM)

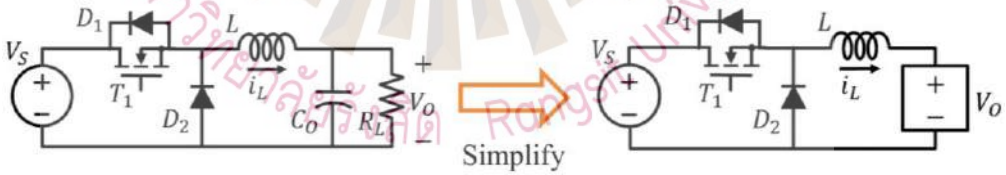
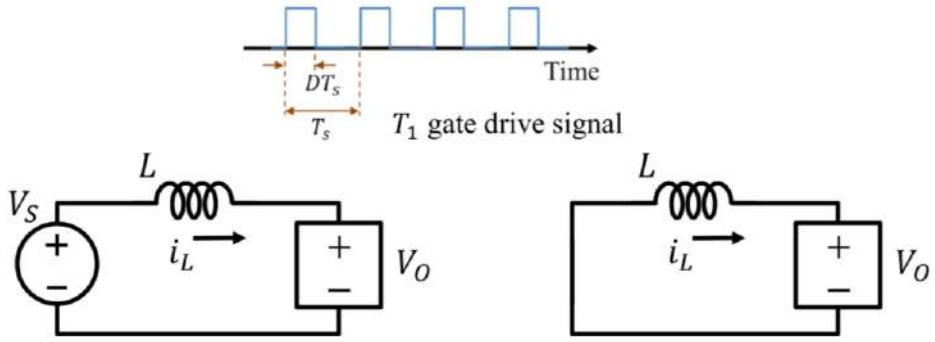


Figure 3.9 Simplified circuit of buck converter circuit

Source: Sooksatra, 2021

Since V_O is assumed to be constant, the output capacitor and load circuit can be replaced by a dc voltage sink denoted by the square block in the right side of Figure 3.9.



When T_1 being turned on: DT_s When T_1 being turned off: $(1-D)T_s$

Figure 3.10 Circuit of buck converter when T_1 being turned on and off

Source: Sooksatra, 2021

During T_1 on: i_L linearly increases with slope $(V_S - V_O)/L$.

During T_1 off: i_L linearly decreases with slope $-V_O/L$.

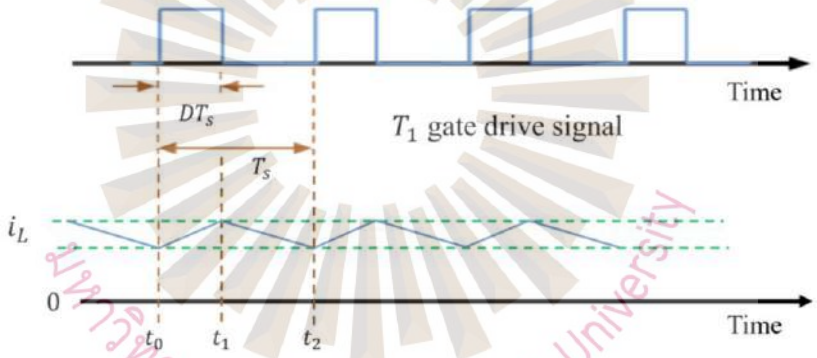


Figure 3.11 Current i_L in time domain of PWM converter in continuous conduction mode

Source: Sooksatra, 2021

Let t_0 be the starting point of the switching period.

$$i_L(t_1) = i_L(t_0) + \frac{V_S - V_O}{L} DT_S \tag{3-8}$$

$$i_L(t_2) = i_L(t_1) - \frac{V_O}{L}(1-D)T_S \tag{3-9}$$

Due to periodicity, $i_L(t_2) = i_L(t_0)$. From equation 3-8 and 3-9, the following relation can be obtained,

$$\frac{V_O}{V_S} = m = D \tag{3-10}$$

which is the converter gain.

Buck converter - Discontinuous conduction mode

When the converter is operated with a light load, i_L may drop to zero during a switching period, and raises up again at the start of the next switching cycle.

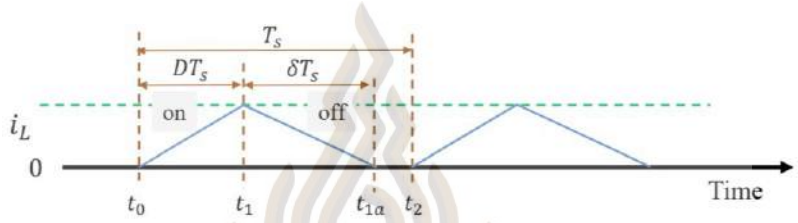


Figure 3.12 Current i_L in time domain of PWM converter in discontinuous conduction mode

Source: Sooksatra, 2021

$$i_L(t_1) = \frac{V_S - V_O}{L} DT_S \tag{3-11}$$

Since $i_L(t_{1a}) = 0$,

$$\delta T_S = t_{1a} - t_1 = \frac{L}{V_O} i_L(t_1) \tag{3-12}$$

Let I_O be the output current, which can be derived from

$$I_O = \frac{1}{T_s} \int_{t_0}^{t_{1a}} i_L dt \tag{3-13}$$

From equations 3-11, 3-12 and 3-13, the expression for I_O can be obtain as

$$I_O = \frac{DT_s}{2L} (V_S - V_O)(D + \delta) \tag{3-14}$$

From Figure 3.12, the converter is operated in DCM under the following condition,

$$\delta < 1 - D \qquad \text{or} \qquad D + \delta < 1$$

Hence, the following relation can be obtained from equation (3-14)

$$I_O < \frac{DT_s}{2L} (V_S - V_O) \tag{3-15}$$

Or

$$I_{nO} < \frac{D}{2}(1-m) \tag{3-16}$$

Where I_{nO} is the normalized output current and is defined by

$$I_{nO} = \frac{L}{V_S T_S} I_O \tag{3-17}$$

From equations 3-14 and 3-17, the following relation can be obtained,

$$I_{nO} = \frac{D}{2}(1-m)(D+\delta) \tag{3-18}$$

Since the average of v_L must be zero,

$$(V_S - V_O)DT_s - V_O \delta T_s = 0 \tag{3-19}$$

Then

$$\frac{V_O}{V_S} = m = \frac{D}{D+\delta} \tag{3-20}$$

Replacing to equation 3-18, the expression of I_{nO} for DCM can be expressed by

$$I_{nO} = \frac{D\delta}{2} \tag{3-21}$$

AT the boundary between CCM and DCM, $\delta = 1 - D$, so equation 3-21 becomes

$$I_{nO} = \frac{D(1-D)}{2} \tag{3-22}$$

Since $D + \delta < 1$ for DCM, the range of converter gain for this mode can be expressed by

$$\frac{V_O}{V_S} > D \tag{3-23}$$

From equations (3-11), (3-12) and (3-14), the converter gain for DCM can be given by

$$m = \frac{D^2}{D^2 + 2I_{nO}} \tag{3-24}$$

Using equation 3-22, the boundary between CCM and DCM can be plotted and is shown in Figure 3.13.

Using equation 3-24 as the gain function in DCM and $m = D$ for CCM, the control characteristics of Buck Converter for both CCM and DCM can be plotted and given in Figure 3.14.

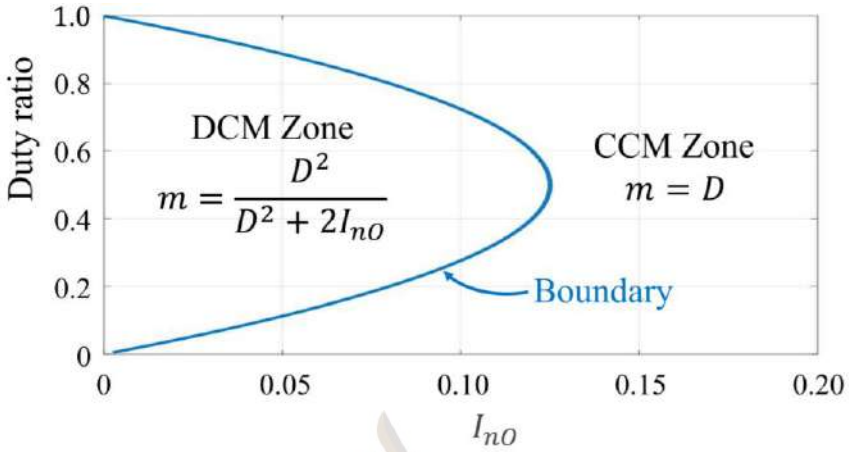


Figure 3.13 Boundary between CCM and DCM on Normalized Output Current and Duty Ratio Plot

Source: Sooksatra, 2021

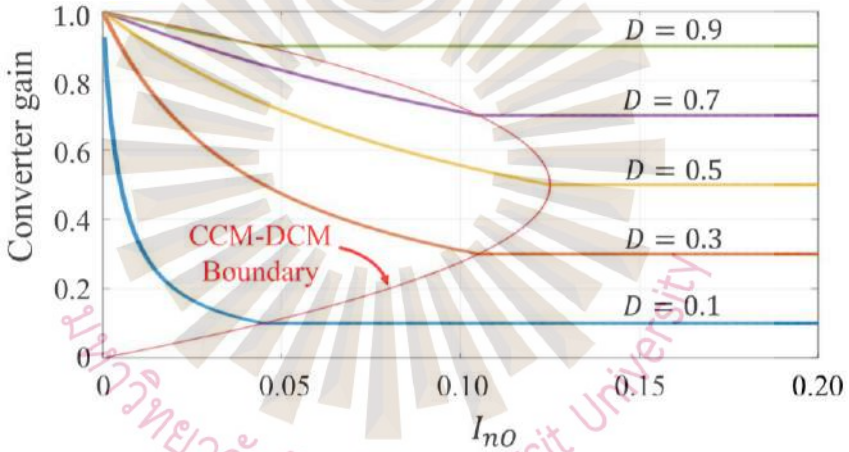


Figure 3.14 Control Characteristics of Buck Converter For both CCM and DCM

Source: Sooksatra, 2021

Boost converter

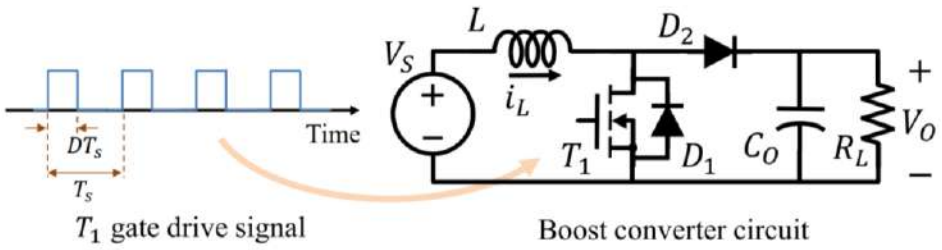


Figure 3.15 Operating gate drive signal for MOSFET T_1 of boost converter circuit

Source: Sooksatra, 2021

Assumption:

1) All devices are assumed to be ideal.

2) MOSFET is turned on and off periodically with period of T_s .

3) During a switching period, T_1 is turned on for DT_s, where is the duty ratio and $0 \leq D \leq 1$.

4) The capacitor is relatively large, so V_O can be assumed constant.

Boost converter - Continuous conduction mode (CCM)

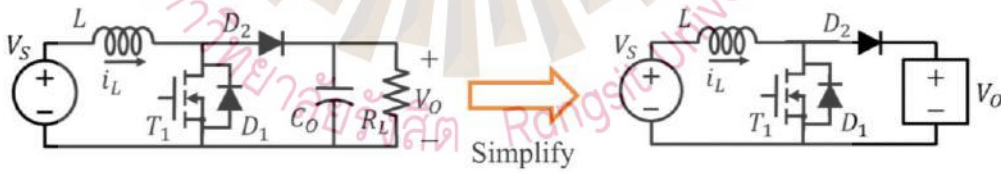
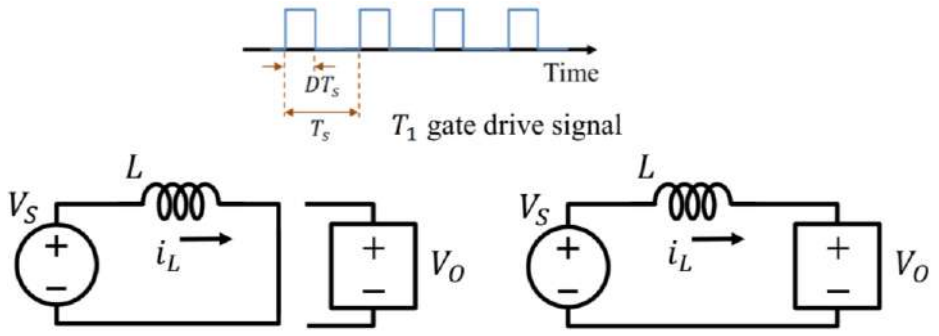


Figure 3.16 Simplified circuit of boost converter circuit

Source: Sooksatra, 2021

Since V_O is assumed to be constant, the output capacitor and load circuit can be replaced by a dc voltage sink denoted by the square block in the right side of Figure 3.16.



When T_1 being turned on: DT_s When T_1 being turned off: $(1-D)T_s$

Figure 3.17 Circuit of boost converter when T_1 being turned on and off

Source: Sooksatra, 2021

During T_1 on: i_L linearly increases with slope V_S/L.

During T_1 off: i_L linearly decreases with slope $(V_S - V_O)/L$.

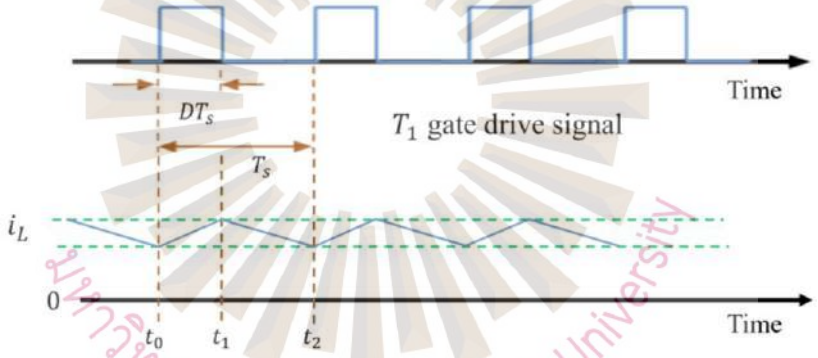


Figure 3.18 Current i_L in time domain of PWM converter in continuous conduction mode

Source: Sooksatra, 2021

Let t_0 be the starting point of the switching period.

$$i_L(t_1) = i_L(t_0) + \frac{V_S}{L} DT_S \tag{3-25}$$

$$i_L(t_2) = i_L(t_1) + \frac{V_S - V_O}{L}(1-D)T_S \tag{3-26}$$

Due to periodicity, $i_L(t_2) = i_L(t_0)$. From equations 3-25 and 3-26, the following relation can be obtained,

$$\frac{V_O}{V_S} = m = \frac{1}{1-D} \tag{3-27}$$

which is the converter gain.

Boost converter - Discontinuous conduction mode

When the converter is operated with a light load, i_L may drop to zero during a switching period, and raises up again at the start of the next switching cycle.

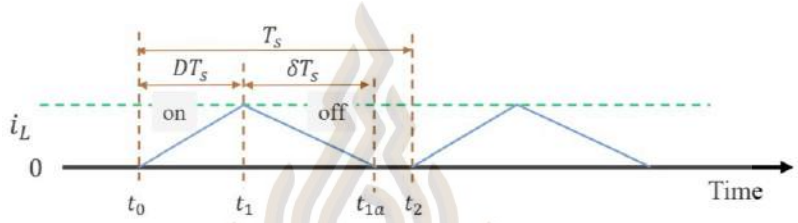


Figure 3.19 Current i_L in time domain of PWM converter in discontinuous conduction mode

Source: Sooksatra, 2021

$$i_L(t_1) = \frac{V_S}{L} DT_S \tag{3-28}$$

Since $i_L(t_{1a}) = 0$,

$$\delta T_S = t_{1a} - t_1 = \frac{L}{V_O - V_S} i_L(t_1) \tag{3-29}$$

Let I_O be the output current, which can be derived from

$$I_O = \frac{1}{T_s} \int_{t_1}^{t_{1a}} i_L dt \tag{3-30}$$

From equations 3-28, 3-29 and 3-30, the expression for I_O can be obtain as

$$I_O = \frac{DT_s}{2L} V_S \delta \tag{3-31}$$

From Figure 3.19, the converter is operated in DCM under the following condition,

$\delta < 1 - D$ or $D + \delta < 1$

Hence, the following relation can be obtained from equation 3-31

$$I_O < \frac{DT_s}{2L} V_S (1 - D) \tag{3-32}$$

Or

$$I_{nO} < \frac{D}{2}(1-D) \tag{3-33}$$

Where I_{nO} is the normalized output current and defined the same as that for Buck Converter,

$$I_{nO} = \frac{L}{V_S T_S} I_O \tag{3-34}$$

From equations 3-31 and 3-34, the following relation can be obtained,

$$I_{nO} = \frac{D\delta}{2} \tag{3-35}$$

Since the average of v_L must be zero,

$$V_S D T_s + (V_S - V_O)\delta T_s = 0 \tag{3-36}$$

Then

$$\frac{V_O}{V_S} = m = \frac{D+\delta}{\delta} \tag{3-37}$$

The above is the converter gain for DCM.

AT the boundary between CCM and DCM, $\delta = 1 - D$, so equation 3-34 becomes

$$I_{nO} = \frac{D(1-D)}{2} \tag{3-38}$$

Since $D + \delta < 1$ for DCM, the range of converter gain for this mode can be expressed by

$$\frac{V_O}{V_S} > \frac{1}{1-D} \tag{3-39}$$

From equations 3-35 and 3-37, the converter gain for DCM can be given by

$$m = \frac{D^2 + 2I_{nO}}{2I_{nO}} \tag{3-40}$$

Using equation 3-38, the boundary between CCM and DCM can be plotted and is shown in Figure 3.20.

Using equation 3-40 as the gain function in DCM and $m = 1/(1-D)$ for CCM, the control characteristics of Buck Converter for both CCM and DCM can be plotted and given in Figure 3.21.

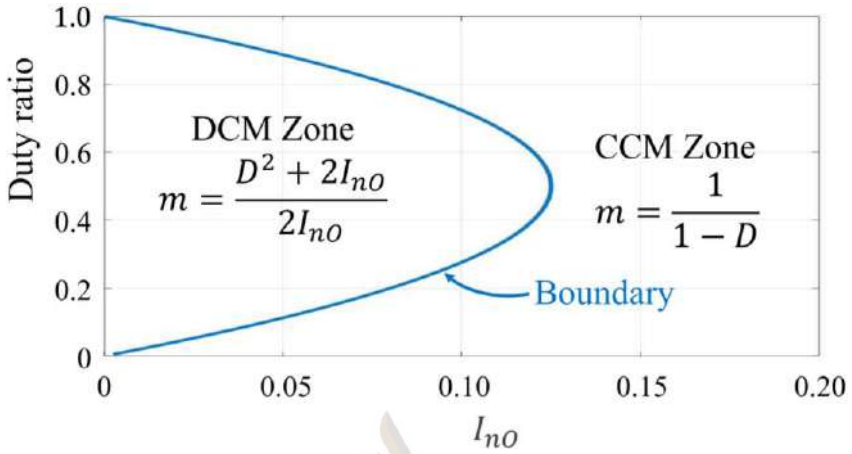


Figure 3.20 Boundary between CCM and DCM on Normalized Output Current and Duty Ratio Plot

Source: Sooksatra, 2021

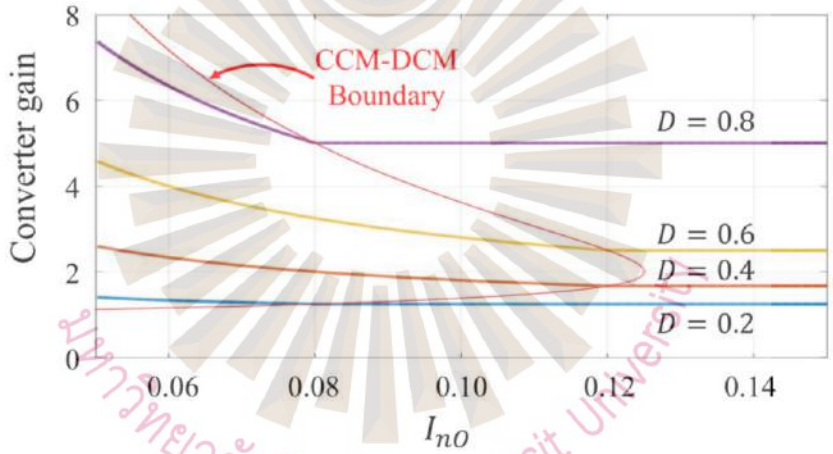


Figure 3.21 Control Characteristics of Boost Converter for both CCM and DCM

Source: Sooksatra, 2021

3.6 Three Portions of Resonant Converter

3.6.1 Source circuit

consisting of source (voltage or current) and MOSFETs.

3.6.2 Resonant tank circuit

consisting of resonant L and C.

3.6.3 Output circuit

consisting of rectifying diodes and load (capacitive or inductive).

3.6.1 Source circuit

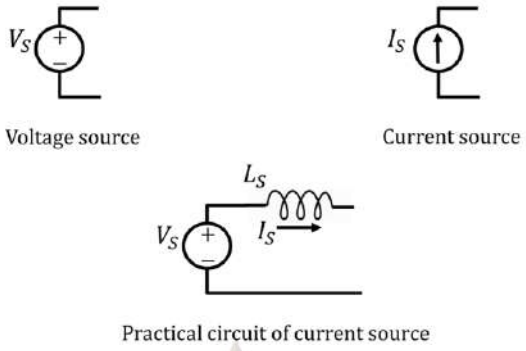


Figure 3.22 Voltage, current and practical circuit of current sources

Source: Sooksatra, 2021

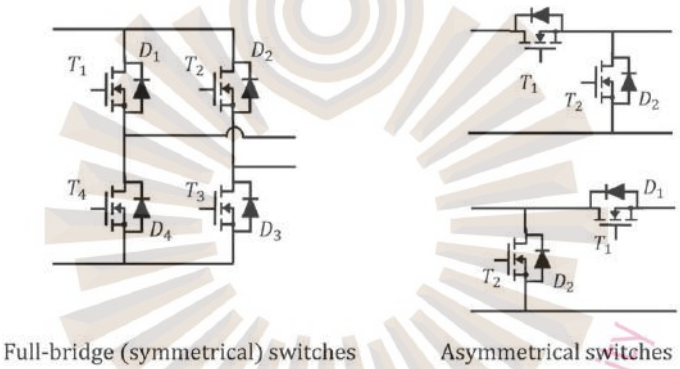


Figure 3.23 Full-bridge (symmetrical) and asymmetrical MOSFETs of source circuit

Source: Sooksatra, 2021

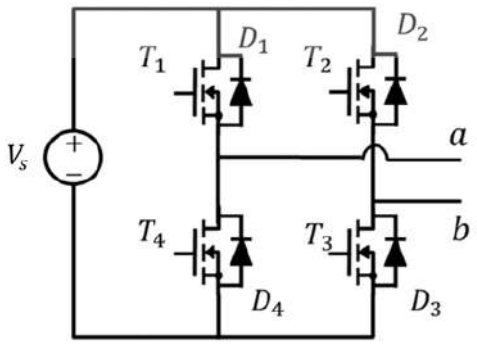


Figure 3.24 Full-bridge MOSFETs connected with voltage source

Source: Sooksatra, 2021

Table 3.1 Voltage of ab terminal from full-bridge MOSFETs connected with voltage source

T_1	T_2	T_3	T_4	*ab* terminal
on	off	on	off	V_s
off	on	off	on	$-V_s$
on	on	off	off	short circuit
off	off	on	on	short circuit
off	off	off	off	open circuit

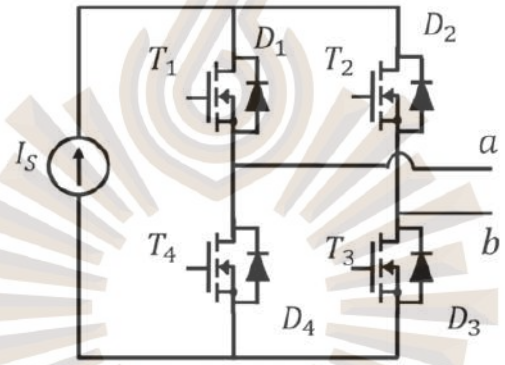


Figure 3.25 Full-bridge MOSFETs connected with current source

Source: Sooksatra, 2021

Table 3.2 Current of ab terminal from full-bridge MOSFETs connected with current source

T_1	T_2	T_3	T_4	*ab* terminal
On	off	on	off	I_s
Off	on	off	on	$-I_s$
On	off	off	on	open circuit
Off	on	on	off	open circuit
On	on	on	on	short circuit

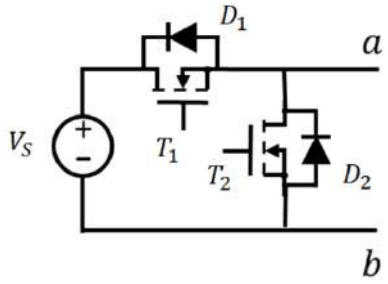


Figure 3.26 Two MOSFETs connected with voltage source

Source: Sooksatra, 2021

Table 3.3 Voltage of ab terminal from two MOSFETs connected with voltage source

T_1	T_2	*ab* terminal
on	off	V_s
off	on	short circuit (0 V)
off	off	open circuit

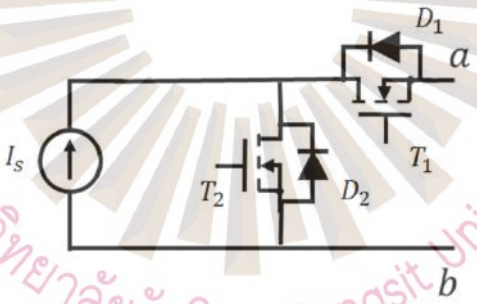


Figure 3.27 Two MOSFETs connected with current source

Source: Sooksatra, 2021

Table 3.4 Current of ab terminal from two MOSFETs connected with current source

T_1	T_2	*ab* terminal
on	off	I_s
off	on	open circuit (0 A)
on	on	short circuit

3.6.2 Resonant tank circuit

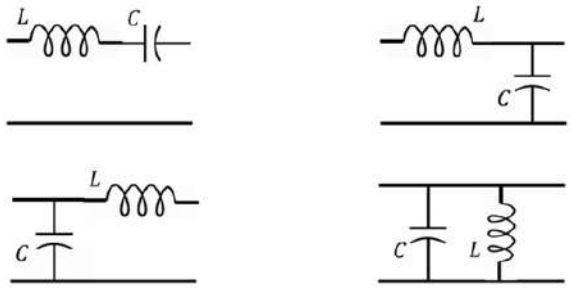


Figure 3.28 Several configurations of LC resonant tank circuit

Source: Sooksatra, 2021

3.6.3 Output circuit

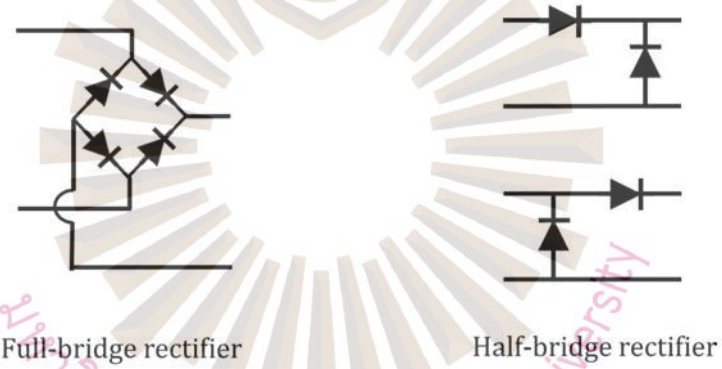


Figure 3.29 Full-bridge and half-bridge rectifier of output circuit

Source: Sooksatra, 2021

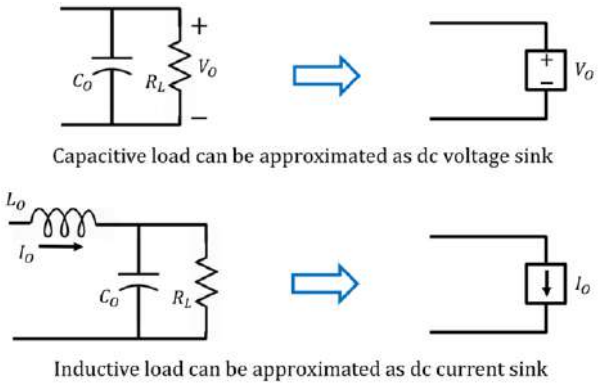


Figure 3.30 Circuit simplification of capacitor directly connected to load and Inductor directly connected to load

Source: Sooksatra, 2021

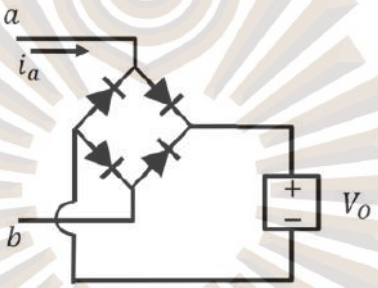


Figure 3.31 Full bridge rectifier connected to voltage sink

Source: Sooksatra, 2021

Table 3.5 Voltage of ab terminal from Full bridge rectifier connected to voltage sink

condition	ab Terminal
$i_a > 0$	V_o
$i_a < 0$	$-V_o$
$i_a = 0$ and $\lvert v_{ab} \rvert < V_o$	open circuit

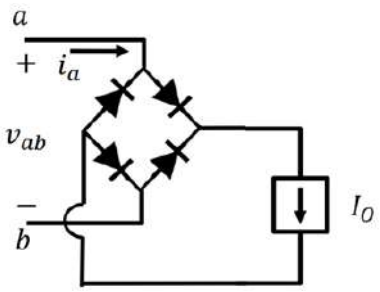


Figure 3.32 Full bridge rectifier connected to current sink

Source: Sooksatra, 2021

Table 3.6 Current of ab terminal from Full bridge rectifier connected to current sink

condition	ab Terminal
$v_{ab} > 0$	I_o
$v_{ab} < 0$	$-I_o$
$v_{ab} = 0$ and $\lvert i_a \rvert < I_o$	short circuit

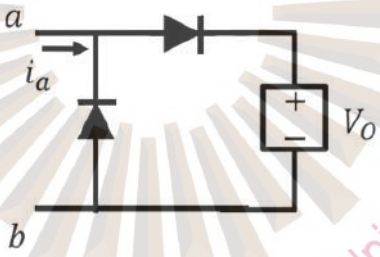


Figure 3.33 Two diode rectifier connected to voltage sink

Source: Sooksatra, 2021

Table 3.7 Voltage of ab terminal from two diode rectifier connected to voltage sink

condition	ab Terminal
$i_a > 0$	V_o
$i_a < 0$	$0\ V$
$i_a = 0$ and $v_{ab} < V_o$	open circuit

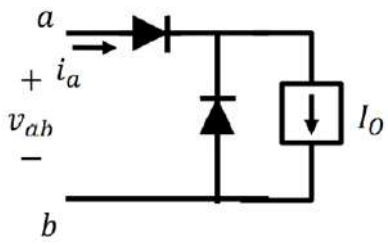


Figure 3.34 Two diode rectifier connected to current sink

Source: Sooksatra, 2021

Table 3.8 Current of ab terminal from two diode rectifier connected to current sink

condition	ab Terminal
$v_{ab} > 0$	I_o
$v_{ab} < 0$	0 A
$v_{ab} = 0$ and $i_a < I_o$	short circuit

3.7 Construction of Resonant Converter

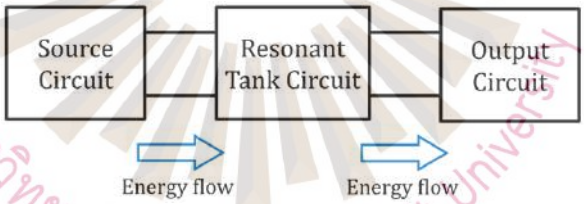


Figure 3.35 Construction of resonant converter

Source: Sooksatra, 2021

3.8 Normalization of LC Circuit Equations

3.8.1 Differential equations for LC circuit

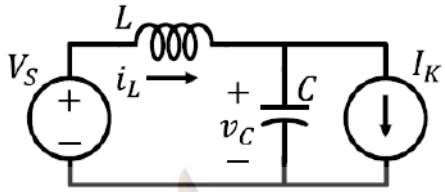


Figure 3.36 An *LC* resonant circuit

Source: Sooksatra, 2021

Considering an *LC* resonant circuit as shown above where V_s and I_K are dc voltage and current sources, respectively, the differential equations can be written as

$$L\frac{di_L}{dt} = V_s - v_c \tag{3-41}$$

$$C\frac{dv_c}{dt} = i_L - I_K \tag{3-42}$$

Then

$$\frac{L}{C}\frac{di_L}{dv_C} = \frac{V_S - v_C}{i_L - I_K} \tag{3-43}$$

The above equation becomes

$$\frac{L}{C}\int (i_L - I_K)di_L = -\int (v_C - V_S)dv_C \tag{3-44}$$

The general solution for the above equation becomes

$$\frac{L}{C}(i_L - I_K)^2 = -(v_C - V_S)^2 + K \tag{3-45}$$

where K is a constant. Having equation 3.45 divided by ${V_S}^2$.

$$\left(\frac{Z_0 i_L}{V_S} - \frac{Z_0 I_K}{V_S}\right)^2 + \left(\frac{v_C}{V_S} - 1\right)^2 = \frac{K}{{V_S}^2} \tag{3-46}$$

In order to have a state-plane diagram represent the resonant *LC* circuit, all parameters must be first normalized. Each voltage and current will be normalized by $\frac{V_S}{Z_0}$ and Z_0, respectively, where

$$Z_0 = \sqrt{\frac{L}{C}} \tag{3-47}$$

Therefore, (3.46) becomes

$$(i_{nL} - I_{nK})^2 + (v_{nC} - 1)^2 = {V_{nm}}^2 \tag{3-48}$$

where i_{nL}, I_{nK} and v_{nC} are the normalized variables of i_L , I_K and v_C, respectively; and

$${V_{nm}}^2 = \frac{M}{{V_S}^2} \tag{3-49}$$

These normalized variables can be expressed by

$$i_{nL} = \frac{Z_o i_L}{V_S} \tag{3-50}$$

$$I_{nK} = \frac{Z_o I_K}{V_S} \tag{3-51}$$

$$v_{nC} = \frac{v_C}{V_S} \tag{3-52}$$

It can be seen from equation 3.48 that trajectory in $v_{nC} - i_{nL}$ plane representing relation between v_{nC} and i_{nL} is a circular curve centered at (1, I_{nK}) with radius = V_{nm}. This trajectory moves in clock-wise direction with angular speed of ω_o, where

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{3-53}$$

The magnitude of V_{nm} depends of the initial values of v_{nC} and i_{nL}. It can be noticed that the time interval from t_i to t_j is directly proportional to the angle under the curve of that portion of time.

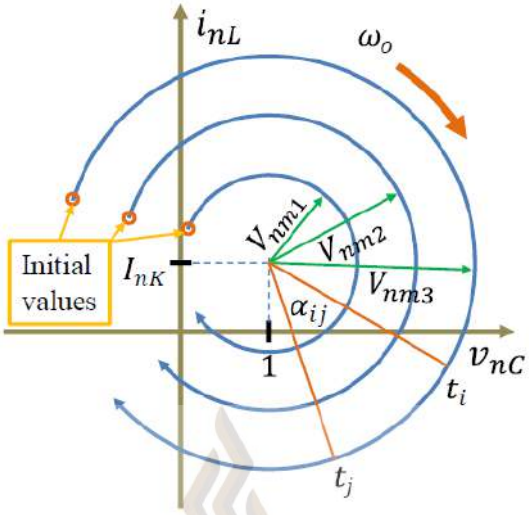


Figure 3.37 The trajectory in v_{nC}-i_{nL} plane representing relation between v_{nC} and i_{nL} is a circular curve centered at (1, I_{nK}) with radius = V_{nm}

Source: Sooksatra, 2021

According to Figure 3.37,

$$\omega_o(t_j - t_i) = \alpha_{ij} \tag{3-54}$$

From the resonant *LC* circuit given earlier, the state-plane diagram can be constructed by the following steps:

1) Locate the center of the circular trajectory by using normalized value of V_S and I_K, which is (1, I_{nK}).

2) Once initial values are given, the initial point can be located at

3) The radius and starting angle can be derived, respectively, as

$$V_{nm} = \sqrt{(1 - v_{nC}(t_0))^2 + (i_{nL}(t_0) - I_{nK})^2} \tag{3-55}$$

$$\theta = \tan^{-1}\frac{i_{nL}(t_0) - I_{nK}}{1 - v_{nC}(t_0)} \tag{3-56}$$

As V_{nm} and θ have been derived and obtained, the responses in time for i_{nL} and v_{nC} can be derived and obtained, respectively, by the following relations,

$$i_{nL}(t) = I_{nK} + V_{nm}\sin[\omega_0(t - t_0) + \theta] \tag{3-57}$$

$$v_{nC}(t) = 1 - V_{nm}\cos[\omega_0(t - t_0) + \theta] \tag{3-58}$$

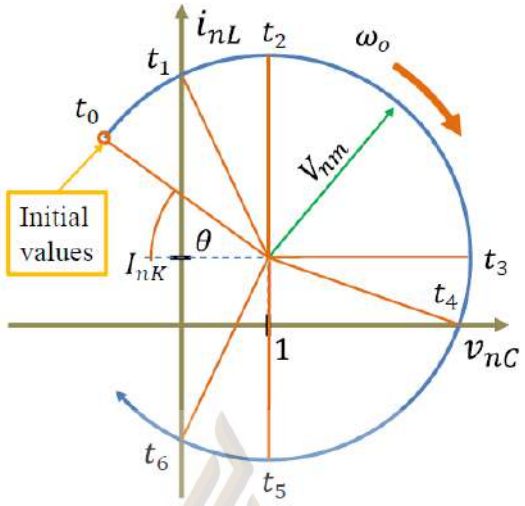


Figure 3.38 The time spots shown in the state-plane diagram

Source: Sooksatra, 2021

As the time spots shown in the state-plane diagram, these time spots can be described as

t_1 : the time that v_C becomes zero,

t_2 : the time that i_L is maximum,

t_3 : the time that v_C is maximum,

t_4 : the time that i_L becomes zero,

t_5 : the time that i_L is minimum,

t_6 : the time that v_C becomes zero again.

By using the obtained state-plane diagram and some properties of trigonometry, t_1 to t_6 can be derived and given, respectively, by the following relations,

$$\omega_0(t_1 - t_0) = \cos^{-1}\frac{1}{V_{nm}} - \theta \tag{3-59}$$

$$\omega_0(t_2 - t_0) = \frac{\pi}{2} - \theta \tag{3-60}$$

$$\omega_0(t_3 - t_0) = \pi - \theta \tag{3-61}$$

$$\omega_0(t_4 - t_0) = \pi + \sin^{-1}\frac{I_{nK}}{V_{nm}} - \theta \tag{3-62}$$

$$\omega_0(t_5 - t_0) = \frac{3\pi}{2} - \theta \tag{3-63}$$

$$\omega_0(t_6 - t_0) = 2\pi - \cos^{-1}\frac{1}{V_{nm}} - \theta \tag{3-64}$$

Energy storage

Energy stored in inductor and capacitor (E_L and E_C) can be expressed, respectively by,

$$E_L = \frac{1}{2}Li_L^2 \tag{3-65}$$

$$E_C = \frac{1}{2}Cv_C^2 \tag{3-66}$$

Using normalized variable at equations 3.65 and 3.66, the total energy stored in resonant LC circuit can be given by

$$E_L + E_C = \frac{CV_s^2}{2}(i_{nL}^2 + v_{nC}^2) \tag{3-67}$$

Since $i_{nL}^2 + v_{nC}^2 = V_E^2$,

$$E_L + E_C \propto V_E^2 \tag{3-68}$$

It can be noticed from equation 3.67 that the total energy stored is directly proportional to V_E^2 where V_E distance from the point on the trajectory to the origin.

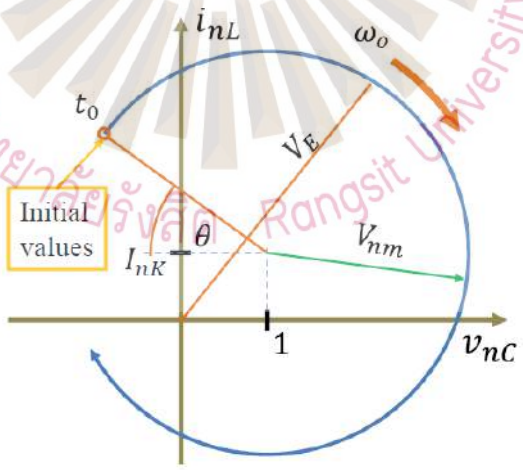


Figure 3.39 The state plane diagram that V_E distance from the point on the trajectory to the origin

Source: Sooksatra, 2021

3.9 Capacitor Voltage Clamping

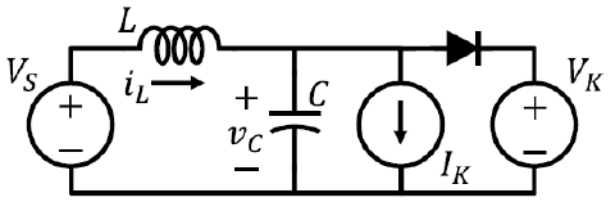


Figure 3.40 An LC resonant circuit as shown above where V_S and V_K are dc voltage sources

Source: Sooksatra, 2021

Considering an LC resonant circuit as shown above where V_S and V_K are dc voltage sources, I_K is a dc current source, it can be seen that v_C cannot be over V_K.

Hence,

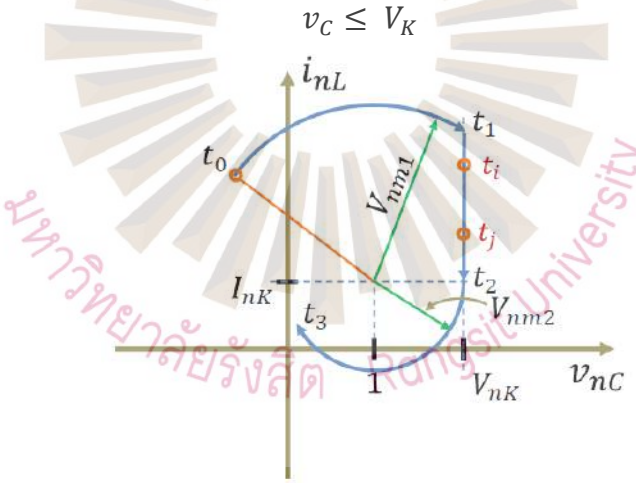
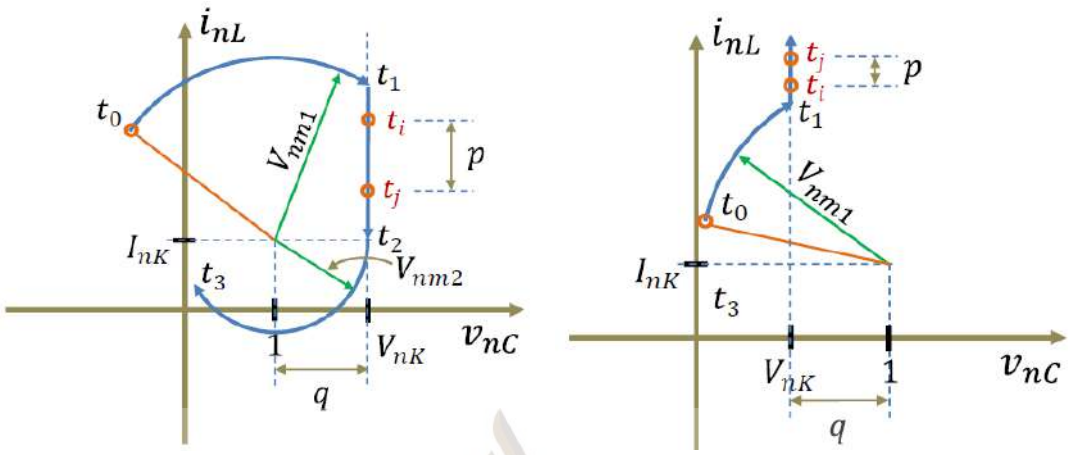


Figure 3.41 The state plane diagram showing Capacitor Voltage Clamping that v_C cannot be over V_K

Source: Sooksatra, 2021



a) $V_K > V_S$ b) $V_K < V_S$

Figure 3.42 Comparing the state plane diagram showing capacitor voltage clamping between a) $V_K > V_S$ and b) $V_K < V_S$

Source: Sooksatra, 2021

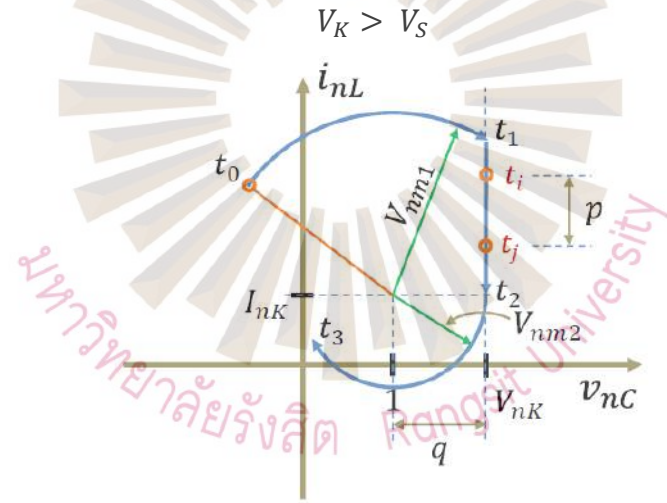


Figure 3.43 The state plane diagram showing Capacitor Voltage Clamping that V_S less than V_K

Source: Sooksatra, 2021

For case: $V_K > V_S$

1) The circuit starts at t_0 where $v_C < V_K$. The circuit resonates until $v_C = V_K$ at t_1.

2) After t_1, v_C is constant at V_K, so decreases linearly due to the constant voltage $(V_S - V_K)$ across the inductor, which is negative.

3) i_L linearly decreases until t_2 where $i_L = I_K$.

4) When $i_L = I_K$ and i_L starts decreasing, C will start discharging, so the circuit starts resonating at t_2.

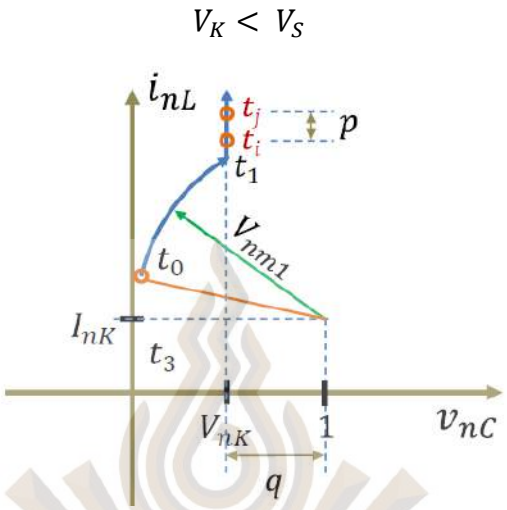


Figure 3.44 The state plane diagram showing capacitor voltage clamping that V_S more than V_K

Source: Sooksatra, 2021

For case: $V_K < V_S$

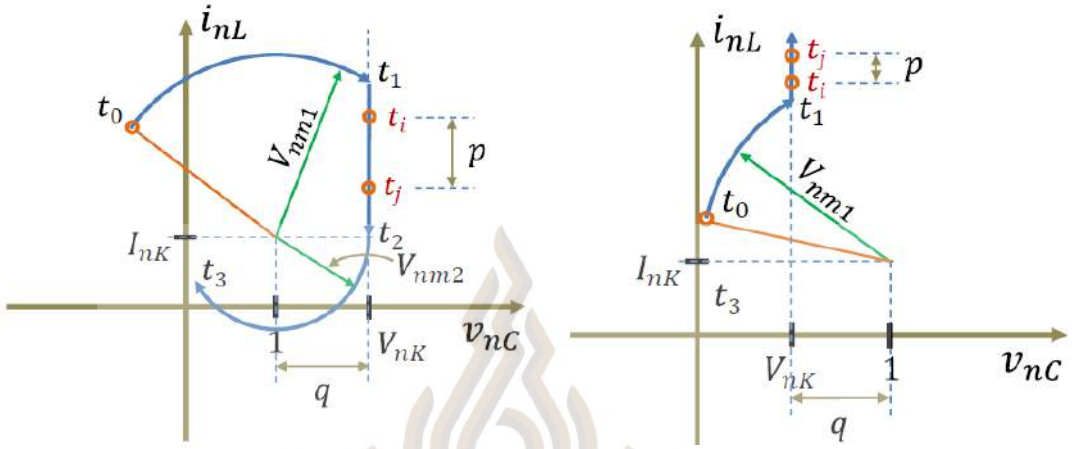
1) The circuit starts at t_0 where $v_C < V_K$. The circuit resonates until at $v_C = V_K$ at t_1.

2) After t_1, v_C is constant at V_K, so i_L increases linearly due to the constant voltage $(V_S - V_K)$ across the inductor, which is positive.

3) i_L will keep increasing linearly if nothing is changed in the circuit.

Calculating time interval during linear change of i_L

Assuming that $t_i < t_j$



a) $V_K > V_S$ b) $V_K < V_S$

Figure 3.45 Comparing the state plane diagram showing capacitor voltage clamping between a) $V_K > V_S$ and b) $V_K < V_S$

Source: Sooksatra, 2021

$$\omega_0(t_j - t_i) = \frac{p}{q} \tag{3-69}$$

From the property of an inductor

$$L\frac{di_L}{dt} = v_L \tag{3-70}$$

Since v_L is constant, so the equation becomes

$$L\frac{\Delta i_L}{\Delta t} = V_s - V_K \tag{3-71}$$

$$L\frac{\Delta di_{nL}}{Z_0 \Delta t} = 1 - V_{nK} \tag{3-72}$$

Then

$$\omega_0 \Delta t = \frac{\Delta i_{nL}}{1 - V_{nK}} \tag{3-73}$$

For $V_s > V_K$ (as in Figure 3.43),

$$\omega_0(t_j - t_i) = \frac{i_{nL}(t_j) - i_{nL}(t_i)}{1 - V_{nK}} \tag{3-74}$$

Using parameters in Figure 3.43,

$$\omega_0(t_j - t_i) = \frac{p}{q} \tag{3-75}$$

As calculated above in case of $V_s > V_K$, we will use equation 3.75 to calculate time interval during linear change of i_L.

For $V_s < V_K$ (as in Figure 3.44),

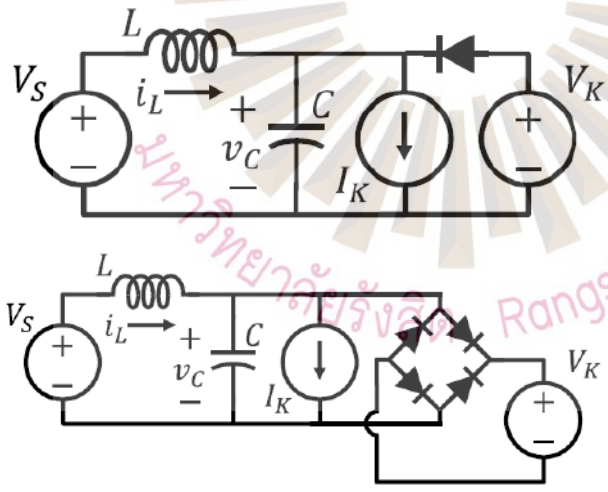
$$\omega_0(t_j - t_i) = \frac{i_{nL}(t_j) - i_{nL}(t_i)}{1 - V_{nK}} \tag{3-76}$$

Using parameters in Figure 3.44,

$$\omega_0(t_j - t_i) = \frac{p}{q} \tag{3-77}$$

As calculated above in case of $V_s < V_K$, we will use equation 3.77 to calculate time interval during linear change of i_L.

More possibilities of capacitor voltage clamping



$v_C \geq V_K$

$-V_K \leq v_C \leq V_K$

Figure 3.46 The resonant circuits of other possible capacitor voltage clamping

Source: Sooksatra, 2021

3.10 Inductor Current Clamping

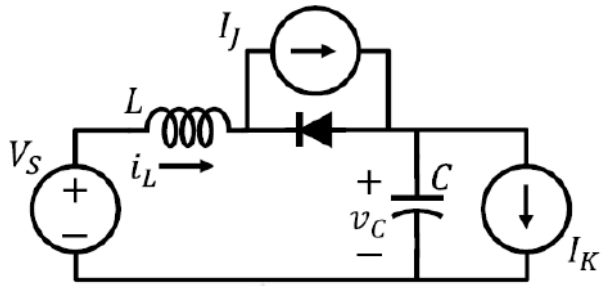


Figure 3.47 an LC resonant circuit as shown above where V_s is dc voltage source, and I_K and I_j are dc current sources

Source: Sooksatra, 2021

Considering an LC resonant circuit as shown above where V_s is dc voltage source, and I_K and I_j are dc current sources, it can be seen that i_L cannot be over I_j.

Hence,

$$i_L \leq I_j$$

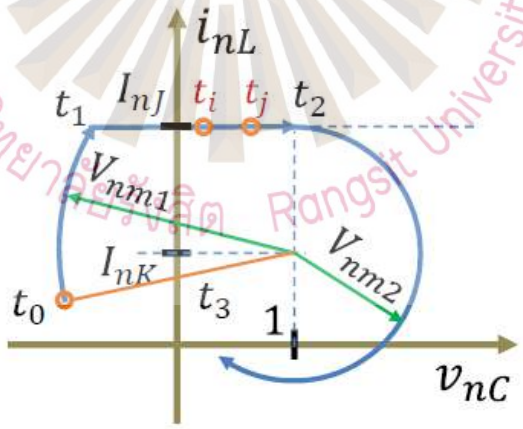
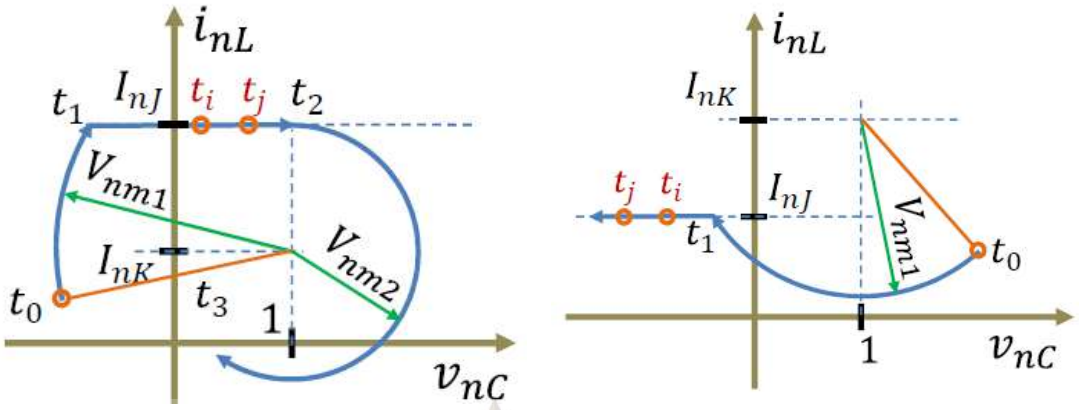


Figure 3.48 The state plane diagram showing inductor current clamping that i_L cannot be over I_j

Source: Sooksatra, 2021



a) $I_j > I_K$ b) $I_j < I_K$

Figure 3.49 Comparing the state plane diagram showing inductor current clamping, a) $I_j > I_K$ and b) $I_j < I_K$

Source: Sooksatra, 2021

$I_j > I_K$

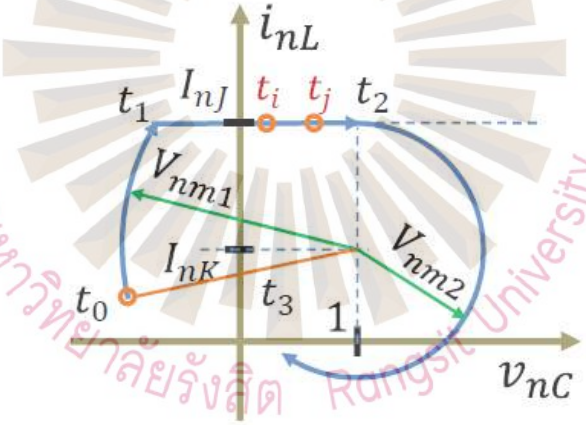


Figure 3.50 The state plane diagram showing inductor current clamping that I_K less than I_j

Source: Sooksatra, 2021

For case: $I_j > I_K$

1) The circuit starts at where $i_L < I_j$. The circuit resonates until $i_L = I_j$ at t_1.

2) After t_1, i_L is constant at I_j, so v_C increases linearly due to the constant current $(I_j - I_K)$ injected to the capacitor.

3) v_C linearly increases until t_2 where $v_C = 1$.

4) When $v_C = V_s$ and v_C starts increasing, will start having negative voltage across it, so the circuit starts resonating at t_2.

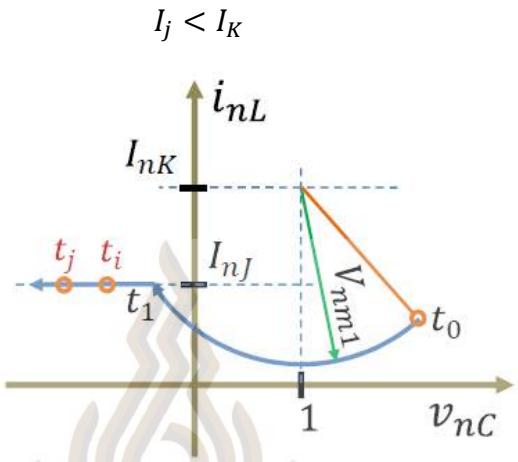


Figure 3.51 The state plane diagram showing inductor current clamping that I_K more than I_j

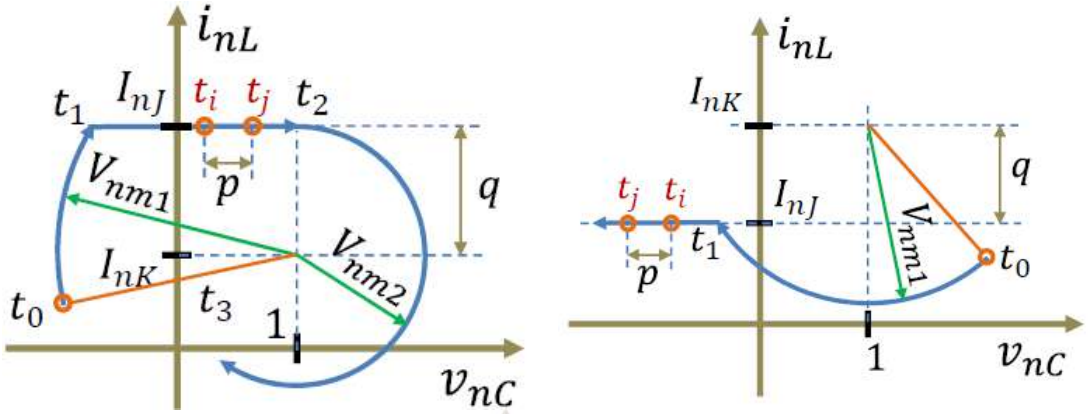
Source: Sooksatra, 2021

For case: $I_j < I_K$

1) The circuit starts at t_0 where $I_L < I_j$. The circuit resonates until $i_L = I_j$ at t_1.

2) After t_1, i_L is constant at I_j, so v_C decreases linearly due to the constant current $(I_K - I_j)$ discharging from the capacitor.

3) v_C will keep decreasing linearly if nothing is changed in the circuit.



a) $I_j > I_K$ b) $I_j < I_K$

Figure 3.52 Comparing the state plane diagram showing inductor current clamping, a) $I_j > I_K$ and b) $I_j < I_K$

Source: Sooksatra, 2021

Calculating time interval during linear change of v_C

From the property of capacitor

$$C\frac{dv_C}{dt} = i_C \tag{3-78}$$

Since i_C is constant, so the equation becomes

$$C\frac{\Delta v_C}{\Delta t} = I_j - I_K \tag{3-79}$$

$$C\frac{\Delta v_{nC}}{\Delta t} = \frac{1}{Z_0}(I_{nj} - I_{nK}) \tag{3-80}$$

Then

$$\omega_0 \Delta t = \frac{\Delta v_{nC}}{I_{nj} - V_{nK}} \tag{3-81}$$

For $I_j > I_K$ (as in Figure 3.50),

$$\omega_0(t_j - t_i) = \frac{v_{nC}(t_j) - v_{nC}(t_i)}{I_{nj} - V_{nK}} \tag{3-82}$$

Using parameters in Figure 3.50,

$$\omega_0(t_j - t_i) = \frac{p}{q} \tag{3-83}$$

As calculated above in case of $I_j > I_K$, we will use equation 3.83 to calculate time interval during linear change of v_C.

For $I_j < I_K$ (as in Figure 3.51),

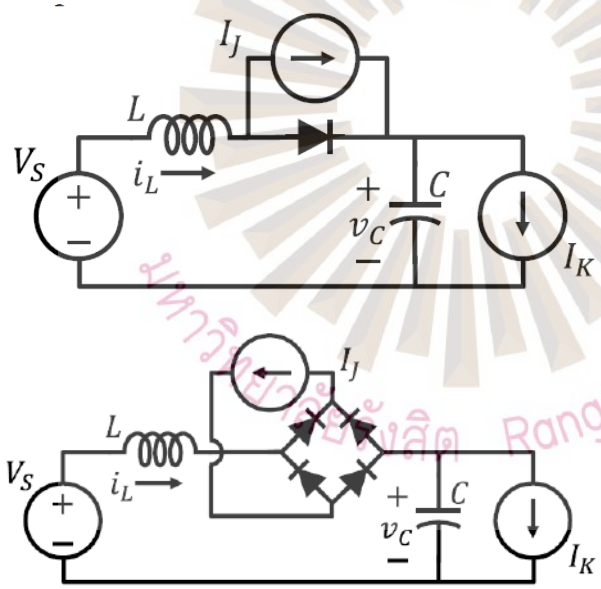
$$\omega_0(t_j - t_i) = \frac{v_{nC}(t_j) - v_{nC}(t_i)}{I_{nj} - V_{nK}} \quad (3\text{-}84)$$

Using parameters in Figure 3.51,

$$\omega_0(t_j - t_i) = \frac{p}{q} \quad (3\text{-}85)$$

As calculated above in case of $I_j < I_K$, we will use equation 3.85 to calculate time interval during linear change of v_C.

More possibilities of inductor current clamping



(a) $I_L \geq I_j$

(b) $-I_j \leq I_L \leq I_j$

Figure 3.53 The resonant circuits of other possible inductor current clamping, a) $I_L \geq I_j$ and b) $-I_j \leq I_L \leq I_j$

Source: Sooksatra, 2021

Chapter 4

Analysis and Design of LCC-Type Zero Voltage Switching Resonant Converter Using State-Plane Diagram

This is LCC-type resonant converter that there is DC voltage source (V_S) connected with asymmetrical switches being source circuit. There are a capacitor (C) connected parallel and both of a capacitor (C_B) and inductor (L) connected series with voltage source being resonant tank circuit. In the part of load circuit, it is composed of full bridge rectifier connected series with an inductor (L_O) and connected parallel with both of a capacitor (C_O) and a resistor (R_L).

Two switches of the source circuit will be turned on and off alternately to generate 10 sequential mode as described in topic 4.1 below.

Because the capacitor (C_B) is rather large so the voltage across will be calculated as constant voltage. The voltage across C_B equal to 0.5*V_S, the state-plane diagram of proposed converter will be symmetrical. The capacitor (C_B) operates as dc blocking device as a definition of a capacitor that average current through a capacitor over a switching period must be zero.

$$\frac{1}{T_s}\int_{t}^{t+T_s} i_C dt = 0$$

Because the output inductor (L_O) is rather large so the output current (I_O) will be calculated as constant current. The output circuit, an inductive load can be approximated as dc current sink as shown in Figure 4.2. The capacitor (C_O) do prevent load change only.

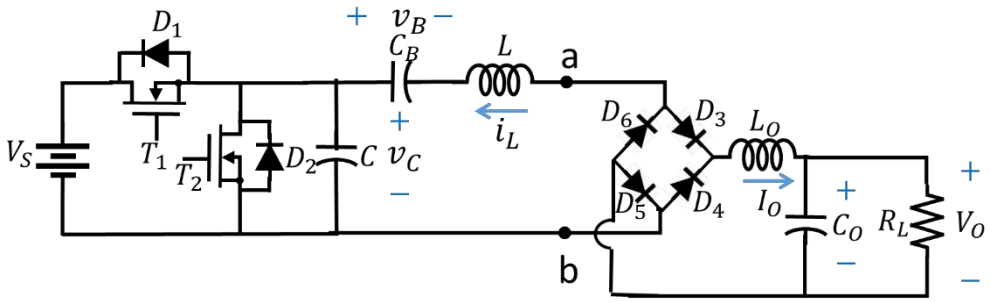


Figure 4.1 Circuit diagram of LCC-type zero voltage switching resonant converter

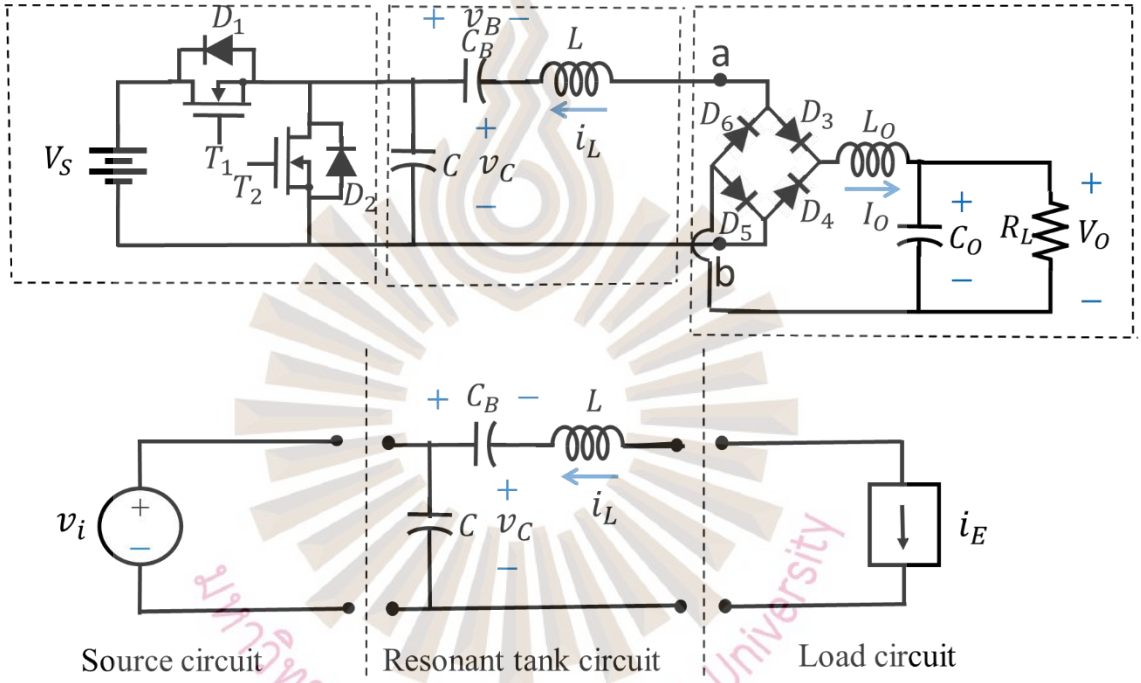


Figure 4.2 Equivalent circuit diagram of the converter with voltage source, resonant tank circuit and load circuits, respectively

4.1 Equivalent Circuit for each Sequential Mode

The following Figures (Figures 4.3-4.12) show the equivalent circuit of each sequential mode from sequential mode 1 to sequential mode 10, respectively.

According to Figure 4.2, v_i will be V_S, short circuit (0 volt) and open circuit depend on a following condition of MOSET T_1 and T_2.

v_i will be V_S when MOSET T_1 is turned on and MOSFET T_2 is turned off.

v_i will be short circuit (0 volt) when MOSFET T_1 is turned off and MOSFET T_2 is turned on.

v_i will be open circuit when MOSFET T_1 is turned off and MOSFET T_2 is turned off.

According to Figure 4.2, i_L is clamped by I_O and $-I_O$. So i_E will be I_O, $-I_O$ and short circuit depend on a following condition of v_{ab} and $|i_L|$.

i_E will be I_O when $v_{ab} > 0$

i_E will be $-I_O$ when $v_{ab} < 0$

i_E will be short circuit when $v_{ab} = 0$ and $|i_L| < I_O$

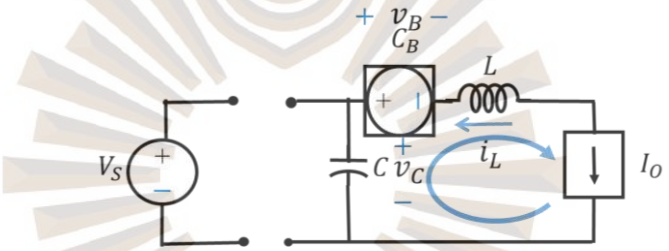


Figure 4.3 Equivalent circuit of sequential mode 1, $t_0 \leq t < t_1$

1) The converter is in sequential mode 1.

2) The switching cycle starts at t_0 when both MOSFET T_1 and T_2 are tuned off.

3) v_C discharges constantly by I_O until $v_C = 0.5 * V_S$ at t_1 and i_L is clamped constantly at I_O.

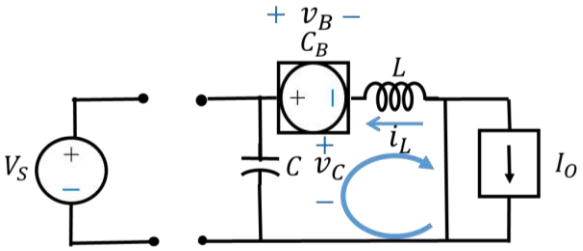


Figure 4.4 Equivalent circuit of sequential mode 2, $t_1 \leq t < t_2$

1) The converter is in sequential mode 2.

2)The sequential mode starts at t_1 when both MOSFET T_1 and T_2 are still turned off.

3) v_C and i_L change resonantly until v_C reaches zero at t_2.

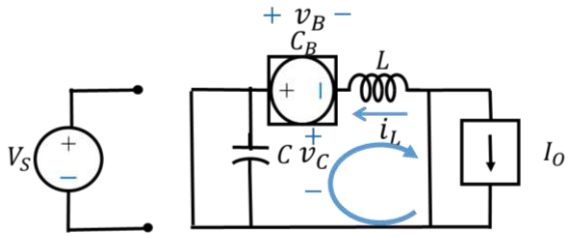


Figure 4.5 Equivalent circuit of sequential mode 3, $t_2 \leq t < t_3$

1) The converter is in sequential mode 3.

2) The sequential mode starts at t_2 when T_1 is still turned off and T_2 is turned on.

3) v_C is clamped constantly at zero and i_L increases linearly until $i_L = 0$ at t_3.

4) T_2 must be turned on during this interval for making the circuit being zero voltage switching circuit.

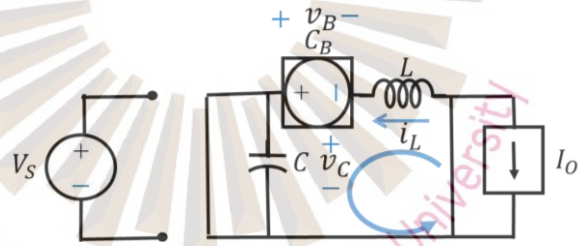


Figure 4.6 Equivalent circuit of sequential mode 4, $t_3 \leq t < t_4$

1) The converter is in sequential mode 4.

2) The sequential mode starts at t_3 when T_1 is still turned off and T_2 is still turned on.

3) v_C is still clamped constantly at zero and i_L increases linearly until $i_L = I_O$ at t_4.

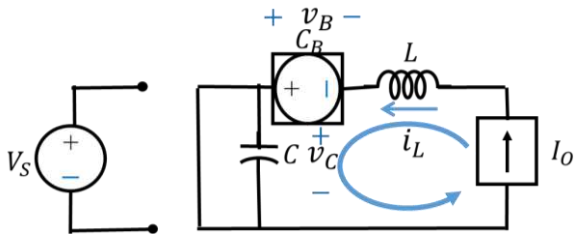


Figure 4.7 Equivalent circuit of sequential mode 5, $t_4 \leq t < t_5$

1) The converter is in sequential mode 5.

2) The sequential mode starts at t_4 when T_1 is still turned off and T_2 is still turned on.

3) v_C is still clamped constantly at zero and $i_L = I_O$.

4) This interval is dead time interval and ends at t_5.

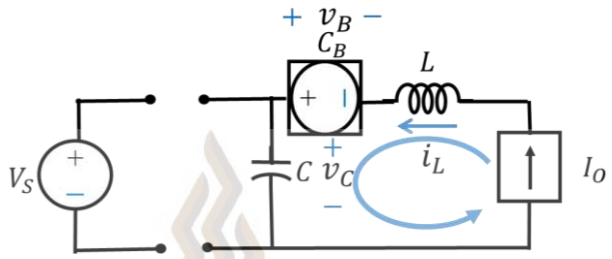


Figure 4.8 Equivalent circuit of sequential mode 6, $t_5 \leq t < t_6$

1) The converter is in sequential mode 6.

2) The sequential mode starts at t_5 when both MOSFET T_1 and T_2 are still turned off.

3) v_C is charged constantly by $-I_O$ until $v_C = 0.5 * V_S$ at t_6 and i_L is clamped constantly at $-I_O$.

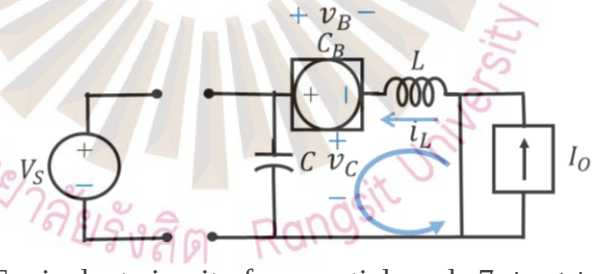


Figure 4.9 Equivalent circuit of sequential mode 7, $t_6 \leq t < t_7$

1) The converter is in sequential mode 7

2) The sequential mode starts at t_6 when both MOSFET T_1 and T_2 are still turned off.

3) v_C and i_L change resonantly until v_C reaches V_S at t_7.

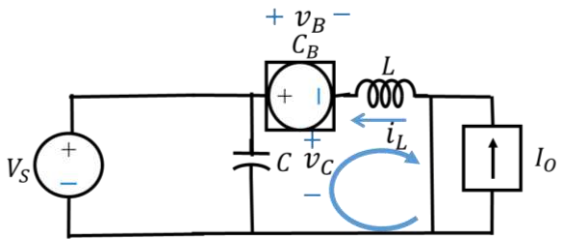


Figure 4.10 Equivalent circuit of sequential mode 8, $t_7 \leq t < t_8$

1) The converter is in sequential mode 8.

2) The sequential mode starts at t_7 when T_1 is turned on and T_2 is still turned off.

3) v_C is clamped constantly at V_S and i_L decreases linearly until $i_L = 0$ at t_8.

4) T_1 must be turned on during this interval for making the circuit being zero voltage switching circuit.

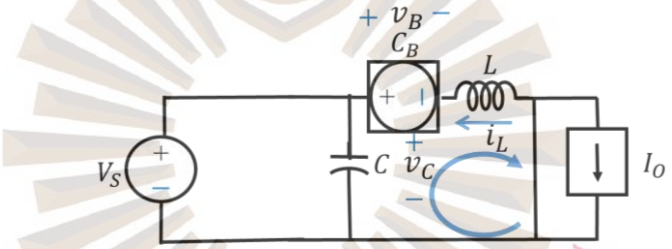


Figure 4.11 Equivalent circuit of sequential mode 9, $t_8 \leq t < t_9$

1) The converter is in sequential mode 9.

2) The sequential mode starts at t_8 when T_1 is still turned on and T_2 is still turned off.

3) v_C is still clamped constantly at V_S and i_L decreases linearly until $i_L = -I_O$ at t_9.

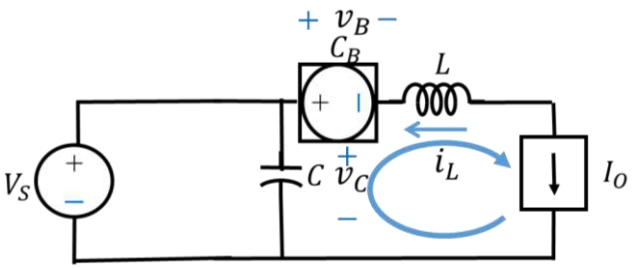


Figure 4.12 Equivalent circuit of sequential mode 10, $t_9 \leq t < t_0 + T_s$

1) The converter is in sequential mode 10.

2) The sequential mode starts at t_9 when T_1 is still turned on and T_2 is still turned off.

3) v_C is still clamped constantly at 0 and $i_L = -I_O$.

4) This interval is dead time interval and ends at $t_0 + T_s$.

5) This interval ends at the end of switching cycle.

4.2 Steady State Analysis of the Proposed Converter

The steady state operation of the purpose converter is analyzed by the state-plane diagram approach. In order to proceed, the following variables need to be normalized.

1) Z_o (characteristic impedance) is square root of L (resonant inductor) divided by C (resonant capacitor).

$$Z_o = \sqrt{\frac{L}{C}} \tag{4-1}$$

2) f_o (natural frequency) is the natural angular speed of the resonant tank circuit divided by 2π.

$$f_o = \frac{\omega_o}{2\pi} = \frac{1}{2\pi\sqrt{LC}} \tag{4-2}$$

3) ω_o (natural angular speed) is given below.

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{4-3}$$

4) i_L (inductor current) is normalized by $\frac{V_s}{Z_o}$ equal to i_{nL}.

$$i_{nL} = \frac{Z_o i_L}{V_s} \tag{4-4}$$

5) I_O (output current) is normalized by $\frac{V_s}{Z_o}$ equal to I_{nO}.

$$I_{nO} = \frac{Z_o I_O}{V_s} \tag{4-5}$$

6) v_C (capacitor voltage across C) is normalized by V_s (source voltage) equal to v_{nC}.

$$v_{nC} = \frac{v_C}{V_s} \tag{4-6}$$

7) V_B(capacitor voltage across C_B) is normalized by V_s (source voltage) equal to V_{nB}.

$$V_{nB} = \frac{V_B}{V_s} \tag{4-7}$$

8) V_O (output voltage) is normalized by V_s (source voltage) equal to V_{nO} (or m).

$$V_{nO} = \frac{V_o}{V_s} = m \tag{4-8}$$

9) f_s (switching frequency) is normalized by f_o equal to f_{ns}.

$$f_{ns} = \frac{f_s}{f_o} \tag{4-9}$$

10) R_L (load resistance) is normalized by Z_o equal to R_{nL}.

$$R_{nL} = \frac{R_L}{Z_o}. \tag{4-10}$$

From the equation of V_{nO}, m is called the converter gain that V_O (output voltage) is normalized by V_s(source voltage).

4.3 State-Plane Diagram Approach

From the equivalent circuit diagram as shown in Figures 4.3-4.12, the ten sequential modes of asymmetrical LCC resonant converter are analyzed by using state-plane diagram approach as shown in Figure 4.13. Because the state-plane diagram presented is symmetrical so only half-time interval of switching period can be calculated for the analysis. From the state-plane diagram presented in Figure 4.13, There are two stationary time interval that are from t_4 to t_5 (in first half-time interval of a switching period) and from t_9 to t_0+T_s (in second half-time interval of a switching period). Limitation of I_{nO} from state-plane diagram shall be more than 0.5 ($I_{nO} > 0.5$) because I_{nO} less than 0.5 will make a resonant curve (t_1 to t_2 and t_6 to t_7) not contact to i_{nl} axis. So a converter cannot operate.

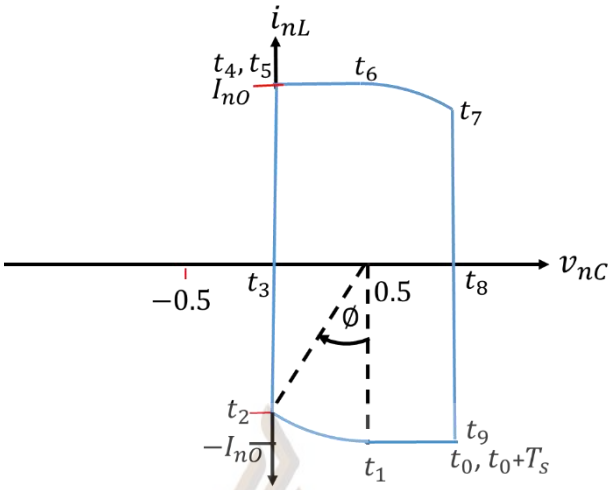


Figure 4.13 State-plane diagram representing steady state operation for the proposed converter

Using the state-plane diagram in Figure 4.13, the normalized inductor current (i_{nL}) and capacitor voltage (v_{nC}) can be calculated in functions of time, respectively, as Sequential mode 1, $t_0 \leq t < t_1$:

$$i_{nL}(t) = -I_{nO}, \tag{4-11}$$

$$v_{nC}(t) = -\omega_o I_{nO}(t - t_o) + 1 \tag{4-12}$$

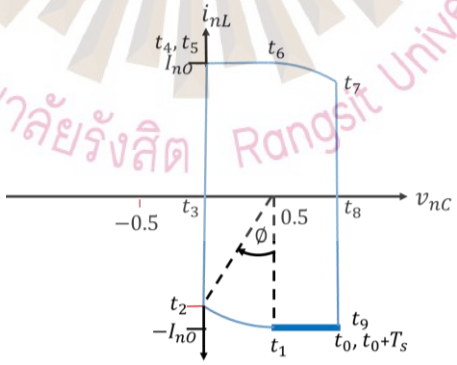


Figure 4.14 State-plane diagram representing steady state operation of the proposed converter for sequential mode 1

Sequential mode 2, $t_1 \leq t < t_2$:

$$i_{nL}(t) = -I_{nO}(\sin(\omega_o(t - t_1) + \frac{\pi}{2})), \tag{4-13}$$

$$v_{nC}(t) = 0.5 + I_{nO}(\cos(\omega_o(t - t_1) + \frac{\pi}{2})) \quad (4\text{-}14)$$

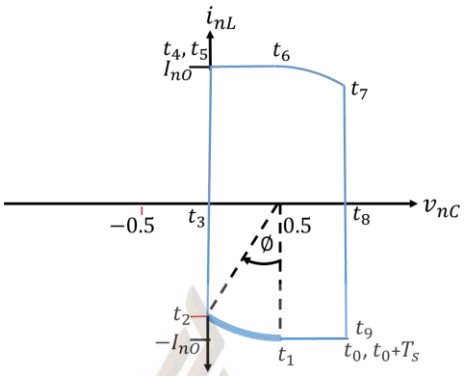


Figure 4.15 State-plane diagram representing steady state operation of the proposed converter for sequential mode 2

Sequential mode 3, $t_2 \leq t < t_3$:

$$i_{nL}(t) = -\sqrt{{I_{nO}}^2 - 0.5^2} + 0.5\omega_o(t - t_2), \quad (4\text{-}15)$$

$$v_{nC}(t) = 0 \quad (4\text{-}16)$$

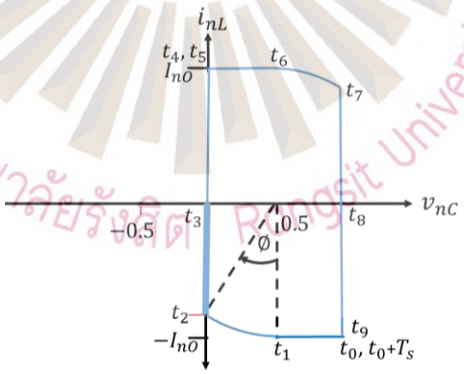


Figure 4.16 State-plane diagram representing steady state operation of the proposed converter for sequential mode 3

Sequential mode 4, $t_3 \leq t < t_4$:

$$i_{nL}(t) = 0.5\omega_o(t - t_3), \quad (4\text{-}17)$$

$$v_{nC}(t) = 0 \quad (4\text{-}18)$$

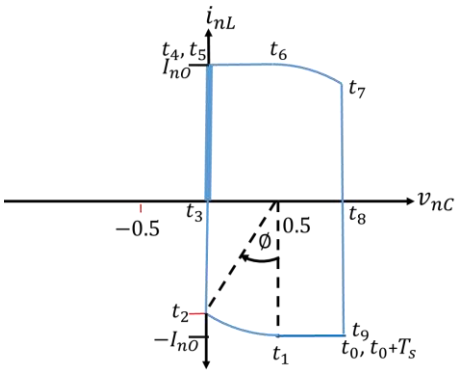


Figure 4.17 State-plane diagram representing steady state operation of the proposed converter for sequential mode 4

Sequential mode 5, $t_4 \leq t < t_5$:

$$i_{nL}(t) = I_{nO}, \tag{4-19}$$

$$v_{nC}(t) = 0 \tag{4-20}$$

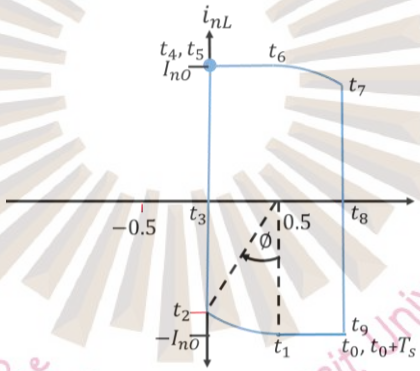


Figure 4.18 State-plane diagram representing steady state operation of the proposed converter for sequential mode 5

Sequential mode 6, $t_5 \leq t < t_6$:

$$i_{nL}(t) = I_{nO}, \tag{4-21}$$

$$v_{nC}(t) = \omega_o I_{nO}(t - t_5) \tag{4-22}$$

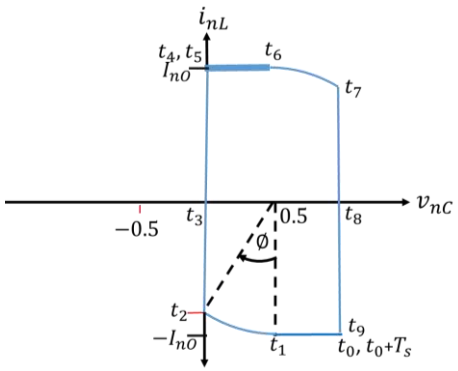


Figure 4.19 State-plane diagram representing steady state operation of the proposed converter for sequential mode 6

Sequential mode 7, $t_6 \leq t < t_7$:

$$i_{nL}(t) = I_{no}(\sin(\omega_0(t - t_6) + \frac{\pi}{2})), \tag{4-23}$$

$$v_{nC}(t) = 0.5 - I_{no}(\cos(\omega_0(t - t_6) + \frac{\pi}{2})) \tag{4-24}$$

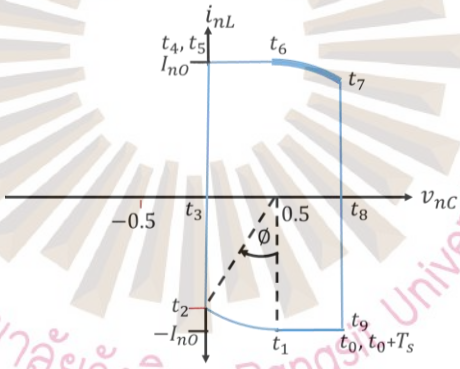


Figure 4.20 State-plane diagram representing steady state operation of the proposed converter for sequential mode 7

Sequential mode 8, $t_7 \leq t < t_8$:

$$i_{nL}(t) = \sqrt{{I_{no}}^2 - 0.5^2} - 0.5\omega_0(t - t_7), \tag{4-25}$$

$$v_{nC}(t) = 1 \tag{4-26}$$

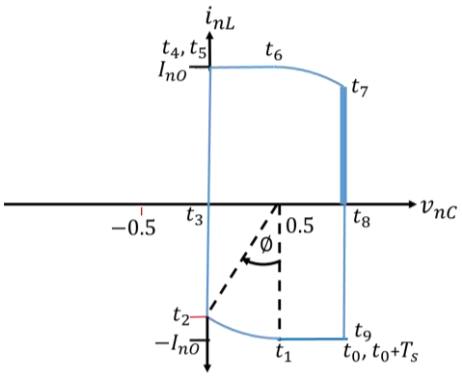


Figure 4.21 State-plane diagram representing steady state operation of the proposed converter for sequential mode 8

Sequential mode 9, $t_8 \leq t < t_9$:

$$i_{nL}(t) = -0.5\omega_0(t - t_8), \tag{4-27}$$

$$v_{nC}(t) = 1 \tag{4-28}$$

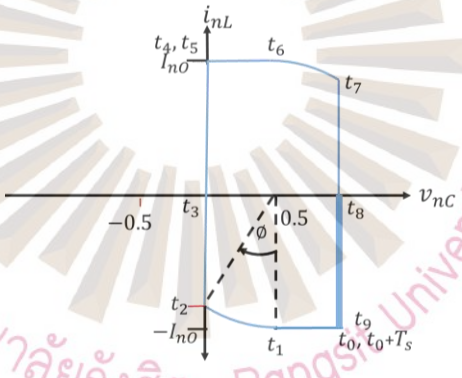


Figure 4.22 State-plane diagram representing steady state operation of the proposed converter for sequential mode 9

Sequential mode 10, $t_9 \leq t < t_0 + T_s$:

$$i_{nL}(t) = -I_{no} \tag{4-29}$$

$$v_{nC}(t) = 1 \tag{4-30}$$

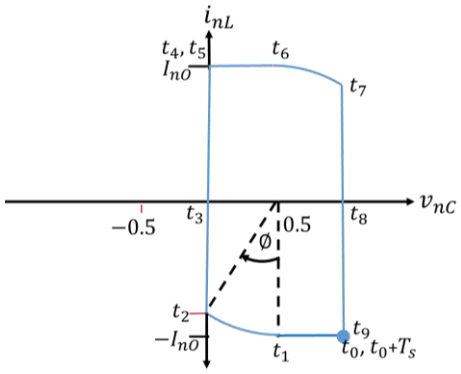


Figure 4.23 State-plane diagram representing steady state operation of the proposed converter for sequential mode 10

From the state-plane diagram, All values of i_{nL} and v_{nC} from equations 4-1 to 4-20 can be simulated versus ωt in OCTAVE program. The simulation of i_{nL} and v_{nC} versus ωt is shown in Figure 4.24.

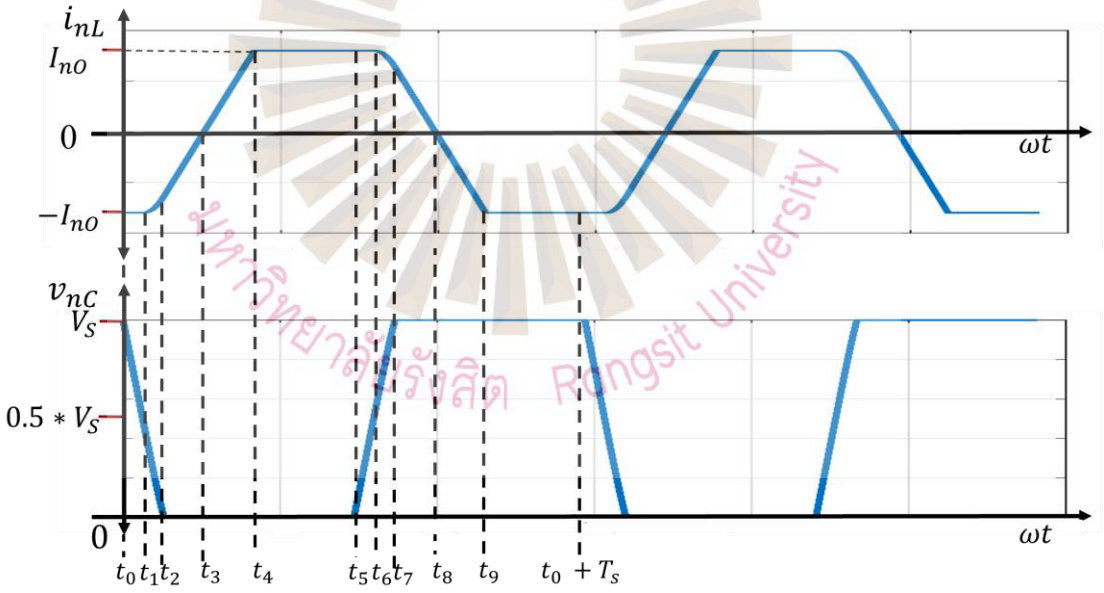


Figure 4.24 Expected waveforms of i_{nL} and v_{nC} derived from state-plane diagram

4.4 Control Characteristics

$$v_C = V_B - v_L + v_{ab} \tag{4-31}$$

Because the average voltage across an inductor (L) over a switching period must be zero according to general concept. So

$$v_{ab} = v_C - V_B \tag{4-32}$$

When v_{ab} more than zero ($v_{ab} > 0$), $i_L = I_O$

When v_{ab} less than zero ($v_{ab} < 0$), $i_L = -I_O$

When v_{ab} equals to zero ($v_{ab} = 0$, short circuit), $|i_L| < I_O$

So $v_{nab} = v_{nC} - V_{nB}$ when $i_L = |I_O|$

From the equivalent circuit of ten sequential modes (Figures 4.3-4.12), There are four Figures (Figures 4.3, 4.7, 4.8 and 4.12) that $i_L = |I_O|$. The remaining Figures (Figures 4.4-4.6 and 4.9-4.11), v_{ab} equals to zero ($v_{ab} = 0$, short circuit), $|i_L| < I_O$.

In order to get the normalized output voltage (V_{nO}) or converter gain (m), It can be calculated from taking average of $|v_{nab}|$ in Figure 4.1. over a switching period.

From $V_B = 0.5 * V_S$, a state-plane diagram of a proposed converter will be symmetrical so only half-time interval over a switching period can be calculated for analysis. The normalized output voltage (V_{nO}) or converter gain (m) can be calculated from only second half-time interval over a switching period, therefore it can be calculated from the equivalent circuit of two sequential modes from t_4 to t_6 (Figures 4.7-4.8).

$$m = v_{nO} = \frac{2}{T_s}\int_{t_4}^{t_6} |v_{nC} - 0.5| dt \tag{4-33}$$

$$\frac{\omega_o T_{s(min)}}{2} = \frac{0.5}{I_{nO}} + \theta + \frac{(I_{nO} + \sqrt{{I_{nO}}^2 - 0.5^2})}{0.5} \tag{4-34}$$

$$\theta = sin^{-1}\frac{0.5}{I_{no}} \tag{4-35}$$

$$\omega_0 T_{dead} = \frac{\omega_0 T_S}{2} - \frac{\omega_0 T_{s(\min)}}{2} \tag{4-36}$$

Replacing v_{nC} from equations 4-10 and 4-12 into 4-21 the function for the converter gain can be derived and given as

$$m = v_{nO} = \frac{2}{T_s}\int_{t_4}^{t_6} |0.5 - v_{nC}|dt \tag{4-37}$$

$$m = \frac{2}{T_s}\left[\int_{t_4}^{t_5} 0.5dt + \int_{t_5}^{t_6} (0.5dt - v_{nC})dt\right] \tag{4-38}$$

Multiplied by $\frac{\omega_0}{\omega_0}$

$$m = \frac{2 * \omega_0}{\omega_0 T_s}\left[0.5T_{dead} + \left(0.5(t_6 - t_5) - \frac{1}{2}(0.5)\left(\frac{0.5}{\omega_0 I_{nO}}\right)\right)\right] \tag{4-39}$$

From $\omega_0 = 2\pi f_0$, $T_s = \frac{1}{f_s}$ and $f_{ns} = \frac{f_s}{f_0}$

$$m = \frac{2 * f_{ns}}{2\pi}\left[0.5\omega_0 T_{dead} + \left(0.5\omega_0\left(\frac{0.5}{\omega_0 I_{nO}}\right) - \frac{0.125}{I_{nO}}\right)\right] \tag{4-40}$$

From $\omega_0 T_{dead} = \frac{\omega_0 T_S}{2} - \frac{\omega_0 T_{s(\min)}}{2}$

$$m = \frac{f_{ns}}{\pi}\left[0.5\left(\frac{\omega_0 T_s}{2} - \frac{\omega_0 T_{s\,min}}{2}\right) + \left(\frac{0.125}{I_{nO}}\right)\right] \tag{4-41}$$

From $\frac{\omega_o T_{s(min)}}{2} = \frac{0.5}{I_{nO}} + \theta + \frac{(I_{nO} + \sqrt{I_{nO}{}^2 - 0.5^2})}{0.5}$ and $\theta = sin^{-1}\frac{0.5}{I_{nO}}$

$$m = \frac{f_{ns}}{\pi}\left[0.5\left\{\frac{\omega_0 T_s}{2} - \left(\frac{0.5}{I_{nO}} + \sin^{-1}\left(\frac{0.5}{I_{nO}}\right) + \left(\frac{I_{nO} + \sqrt{I_{nO}{}^2 - 0.5^2}}{0.5}\right)\right)\right\} + \left(\frac{0.125}{I_{nO}}\right)\right] \tag{4-42}$$

From $\omega_0 = 2\pi f_0, T_s = \frac{1}{f_s}$ and $f_{ns} = \frac{f_s}{f_0}$

$$m = \frac{f_{ns}}{\pi}\left[\frac{0.5\pi}{f_{ns}} - \frac{0.25}{I_{nO}} - 0.5\sin^{-1}\left(\frac{0.5}{I_{nO}}\right) - I_{nO} - \sqrt{I_{nO}{}^2 - 0.5^2} + \left(\frac{0.125}{I_{nO}}\right)\right] \tag{4-43}$$

$$m = \frac{f_{ns}}{\pi}\left[\frac{0.5\pi}{f_{ns}} - \frac{0.125}{I_{nO}} - 0.5\sin^{-1}\left(\frac{0.5}{I_{nO}}\right) - I_{nO} - \sqrt{I_{nO}{}^2 - 0.5^2}\right] \tag{4-44}$$

Using equation 4-44, the simulation result for converter gain versus variable frequency for each current load condition is presented in Figure 4.25 by programming equation in OCTAVE software.

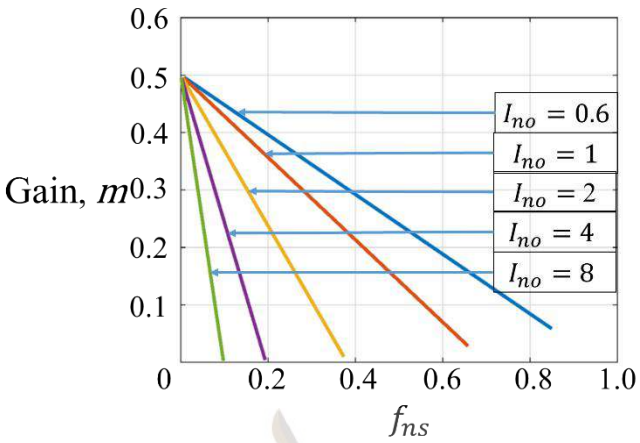


Figure 4.25 The control characteristics of the proposed converter

4.5 Condition for Zero Voltage Switching

From Figure 4.13, a converter is assumed that a switching period starts from t_0 that MOSFET T_1 is just turned off and both MOSFET T_1 and T_2 are off. The MOSFET T_2 must be turned on between t_2 and t_3. There is the turn-off gap between t_0 and t_2. In order to get a turn-off gap. From Figure 4.13 show state-plane diagram of the proposed converter,

$$\omega_0 t = \theta \tag{4-45}$$

$$\omega_0 (t_1 - t_0) = \frac{0.5}{I_{nO}} \tag{4-46}$$

$$\omega_0 (t_2 - t_1) = sin^{-1}\frac{0.5}{I_{nO}} \tag{4-47}$$

$$\omega_0 (t_3 - t_2) = \frac{\sqrt{I_{nO}^2 - 0.5^2}}{0.5} \tag{4-48}$$

So

$$\omega_0 (t_2 - t_0) = \frac{0.5}{I_{nO}} + sin^{-1}\frac{0.5}{I_{nO}} \tag{4-49}$$

$$\omega_0 (t_3 - t_0) = \frac{0.5}{I_{nO}} + sin^{-1}\frac{0.5}{I_{nO}} + \frac{\sqrt{I_{nO}^2 - 0.5^2}}{0.5} \tag{4-50}$$

Using equations 4-49 and 4-50, the curves between $\omega_0 (t_2 - t_0)$ and $\omega_0 (t_3 - t_0)$ versus normalized load current (I_{no}) can be plotted and are shown simultaneously, in Figure 4.26

$\omega_0\,(t_2 - t_0)$ is minimum angle for turning on MOSFET T_2 after turning off MOSFET T_1.

$\omega_0\,(t_3 - t_0)$ is maximum angle for turning on MOSFET T_2 after turning off MOSFET T_1.

From Figure 4.26, $\omega_0\, t = 2.3$ is a recommended value used for calculating zero voltage switching because it stays between minimum and maximum angle (for turning on MOSFET T_2 after turning off MOSFET T_1) for whole range of normalized load current (I_{no}).

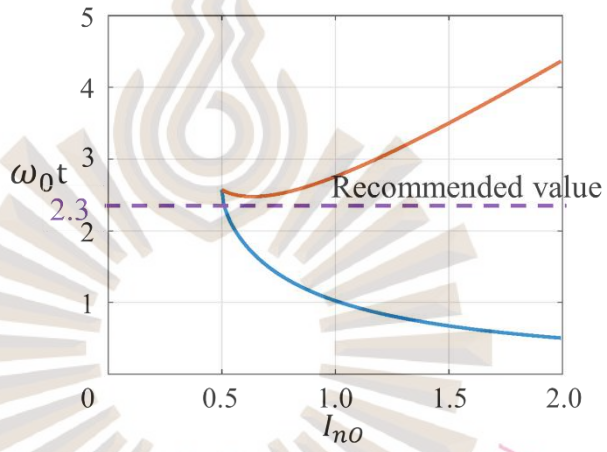


Figure 4.26 The range of $\omega_0\,(t_2 - t_0)$ and $\omega_0\,(t_3 - t_0)$ versus normalized load current (I_{no})

4.6 Design Example and Simulation

$$V_S = 20\text{ V}, \qquad V_O = 6\text{ V},$$
$$I_O = 2\text{ A}, \qquad f_S = 10\text{ kHz}.$$

From the above information,

$$m = \frac{V_O}{V_S} = \frac{6}{20} = 0.3 \tag{4-51}$$

$$R_L = \frac{V_O}{I_O} = \frac{6}{2} = 3\ \Omega \tag{4-52}$$

Selecting $I_{no} = 2$ A. with $m = 0.3$, $f_{ns} = 0.15$ is found in the control characteristic in Figure 4.25

Finding Z_o

$$I_{no} = \frac{Z_o\, I_O}{V_S} \tag{4-53}$$

$$2 = \frac{Z_o\,(2)}{20} \tag{4-54}$$

$$Z_o = 20 \tag{4-55}$$

Finding f_0

$$f_{ns} = \frac{f_s}{f_0} \tag{4-56}$$

$$0.15 = \frac{10\text{ k}}{f_0} \tag{4-57}$$

From $\omega_0 = 2\pi f_0$

$$\frac{1}{\sqrt{LC}} = 2\pi * 66.67\text{ k} \tag{4-58}$$

$$Z_0 = \sqrt{\frac{L}{C}} = 20 \tag{4-59}$$

$$\sqrt{L} = 20\sqrt{C} \tag{4-60}$$

Substitute $\sqrt{L}$ in equation 4-58

$$\frac{1}{20\sqrt{C}\sqrt{C}} = 2\pi * 66.67\text{ k} \tag{4-61}$$

$$C = 0.12\mu\text{F} \tag{4-62}$$

Substitute C in equation 4-60

$$\sqrt{L} = 20\sqrt{0.12\mu} \tag{4-63}$$

$$L = 48\ \mu\text{H} \tag{4-64}$$

i_L must not more than $I_O = 2$ A.

V_B must be half of V_s so

$$V_B = \frac{V_s}{2} = \frac{20}{2} = 10\text{ V} \tag{4-65}$$

Ripple 1% will get

$$\frac{1}{100} * V_B = 0.1 \tag{4-66}$$

$$C_B * \frac{\Delta V_B}{\Delta t} = i_L = 2 \tag{4-67}$$

$$C_B = \frac{0.1\text{m}}{0.1} = 1{,}000\ \mu\text{F} \tag{4-68}$$

Δt will be half of switching period ($f_s = 10$ kHz.) so

$$t_s = \frac{1}{10\text{k}} = 0.1\text{ m} \tag{4-69}$$

$$\Delta t = \frac{t_s}{2} = \frac{0.1\text{ m}}{2} = 0.05\text{ m} \tag{4-70}$$

Finding L_O

$$v_L = 10 - V_O = 4\,V. \tag{4-71}$$

Ripple 1%

$$i_O = \frac{1}{100} * I_O \tag{4-72}$$

$$i_O = \frac{1}{100} * 2 = 0.02\text{ A}. \tag{4-73}$$

$$L_O * \frac{\Delta i_o}{\Delta t} = v_L \tag{4-74}$$

$$L_O * \frac{0.02}{0.05\text{ m}} = 4 \tag{4-75}$$

$$L_O = \frac{0.2\,m}{0.02} = 10\text{ mH}. \tag{4-76}$$

Finding T_{gap}, select $\omega_o T_{gap} = 2.3$ and $f_0 = 66.67$ kHz.

$$\omega_o T_{gap} = 2.3 \tag{4-77}$$

$$T_{gap} = \frac{2.3}{\omega_o} \tag{4-78}$$

$$T_{gap} = \frac{2.3}{2\pi * (66.67\text{ k})} \tag{4-79}$$

$$T_{gap} = 5.49\ \mu\text{s} \tag{4-80}$$

In order to get appropriate ripple at output, the circuit will use $L_O = 10$ mH, $C_B = 1000\ \mu$F and $T_{gap} = 5.49\ \mu$s.

4.7 Simulation Results

Figure 4.27 shows the circuit simulated in PSIM of LCC-Type Zero Voltage Switching Resonant Converter

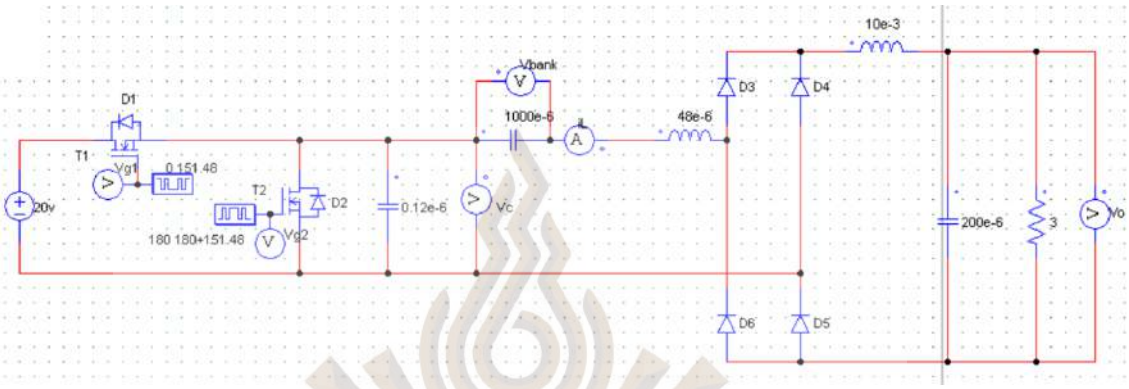


Figure 4.27 The circuit simulated in PSIM of LCC-Type Zero Voltage Switching Resonant Converter

The simulation results from PSIM program in Figures 4.28 and 4.29, Figure 4.28 show initial state from starting point of electrical input to circuit until steady state, while Figure 4.29 shows the simulation result of i_L, v_C v_B, v_{g1} and v_{g2} during steady state operation.

i_L is current of resonant inductor.

v_C is voltage across resonant capacitor.

v_B is voltage across resonant capacitor 1,000 µF.

v_{g1} is gate drive signal for MOSFET T_1.

v_{g2} is gate drive signal for MOSFET T_2.

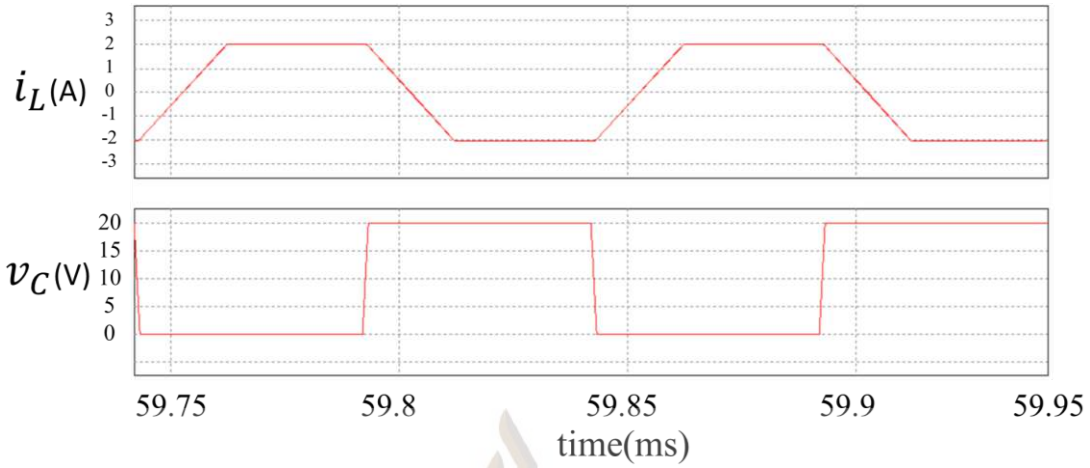


Figure 4.28 Simulation results showing initial state from starting point of electrical input to circuit until steady state

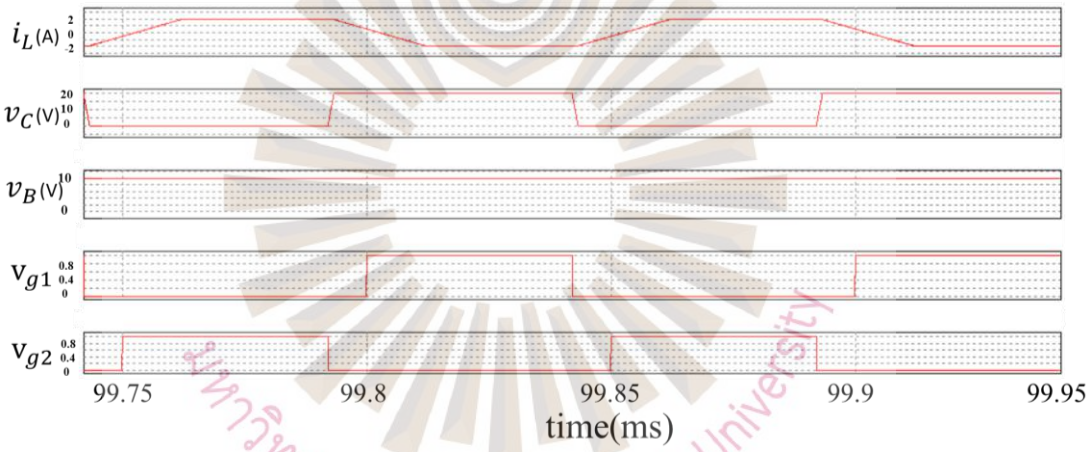


Figure 4.29 The simulation results of i_L, v_C, v_B, v_{g1} and v_{g2} during steady state operation

4.8 Generation of Gate Drive Signals for MOSFETs in the Converter

The logical block diagram for generating gate drive signals to MOSET T_1 and T_2 in converter shown in Figure 4.30. Initially, Voltage-controlled pulse width modulator (PWM)-PWM signal generator (PWM) is an equipment that can generate digital signal to control an analog equipment. Pulse width of PWM is determined as required but maximum voltage for PWM is determined by voltage control. It generates V_g signal. V_g signal is a trigger signal for monostable multi-vibrator. This signal is sent

to monostable multi-vibrator to get V_{bank} signal. Monosatable Multivibrators is a circuit that can generate pulse or square wave from receiving trigger signal externally. Operation of Monosatable Multivibrators is on stable state until getting trigger signal externally. Then it changes to unstable state short time period. Time period is determined by R (resistor) and C (Capacitor) in a circuit of Monosatable Multivibrators.

V_{bank} signal is sent to Toggle flip-flop as clock signal. A toggle flip-flop is normally sequential circuit. It can be defined to toggle with rising edge or falling edge of clock signal. In this case, It will be defined to toggle with rising edge of clock signal (V_{bank}) and T signal are always HIGH state. a toggle flip-flop generates Q and $\overline{Q}$ signal from receiving of V_{bank}.

Q signal is sent to AND gate with $\overline{V}_{bank}$ signal to get gate drive signal for MOSFET T_1

$\overline{Q}$ signal is sent to AND gate with $\overline{V}_{bank}$ signal to get gate drive signal for MOSFET T_2

After getting gate drive signal for MOSFET T_1 and T_2, From Figure 4.31, There are turn off time interval between T_1 and T_2 signal that are determined by the monostable multi-vibrator.

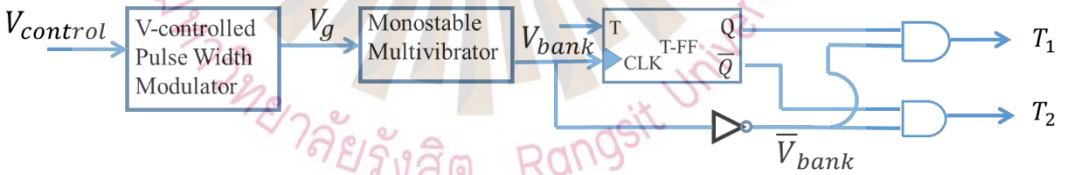


Figure 4.30 The logical block diagram for generating gate drive signals to MOSETs in converter

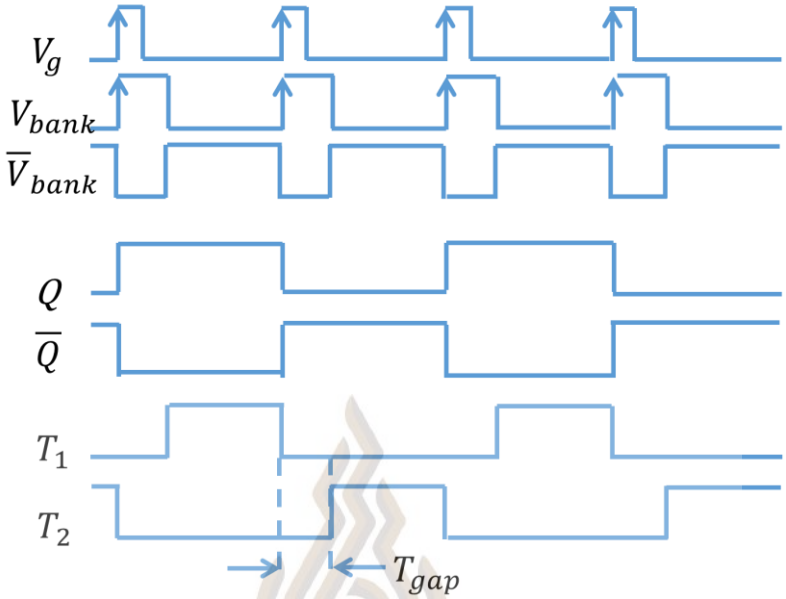


Figure 4.31 Diagram for generating gate drive signals of MOSFET T_1 and T_2

Chapter 5

Conclusion and Recommendations

5.1 Conclusion

A DC to DC proposed converter is analyzed by using state-plane diagram approach in steady state operation. Each current load condition can be controlled output voltage or converter gain by variable frequency.

In load circuit, The average voltage across an inductor over a switching period must be zero during steady state, so the current flows through an inductor will be constant. Then an inductor connected to load can be simplified to a de current sink (I_O). The capacitor C_O in load circuit operates as protecting a load changing.

State-plane diagram approach can only analyze a second order resonant converter. More order resonant converter can not be analyzed by state-plane diagram approach.

1) Using State-Plane Diagram approach make easy to analyze and understand a resonant converter.

2) LCC-Type ZVS Resonant Converter can charge several load conditions by using frequency as a control parameter.

3) Due to Zero voltage switching, a proposed converter will get low loss and minimum size in high frequency.

4) For the proposed converter, several load condition can be changed by using switching frequency as a control parameter.

5) Precise calculation for a second order resonant circuit can be achieved by using State-Plane Diagram approach.

6) Due to Zero voltage switching, an efficiency of a proposed converter will be increased.

5.2 Recommendations

1) Due to C_B equal to 0.5*V_S, the state-plane diagram of proposed converter will be symmetrical.

2) LCC-Type Zero Voltage Switching Resonant Converter can charge different current load equipment in space ship by using variable frequency.

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Appendices

Appendix A

The Programming Codes

```
%The programming codes of each sequential mode programmed
   %in OCTAVE to show State-plane diagram representing
%steady state operation and expected waveforms of inl and
      %vnc in time domain of the proposed converter

cycle=2;                        %create 2 cycle
ino=0.8;                        %determine ino=0.8
beta=acos(0.5/ino);
wt01=0.5/ino;                   %degree of angle from t0 to t1
wt12=(pi()/2)-beta;             %degree of angle from t1 to t2
wt23=sqrt(ino^2-0.5^2)/0.5;%degree of angle from t2 to t3
wt34=ino/0.5;                   %degree of angle from t3 to t4
wt44s=wt34*2;                   %degree of angle from t4 to t5
wt4s5=0.5/ino;                  %degree of angle from t5 to t6
wt56=(pi()/2)-beta;             %degree of angle from t6 to t7
wt67=sqrt(ino^2-0.5^2)/0.5;%degree of angle from t7 to t8
wt78=ino/0.5;                   %degree of angle from t8 to t9
wt88s=wt34*2;                  %degree of angle from t9 to t10
wts=wt01+wt12+wt23+wt34+wt44s+wt4s5+wt56+wt67+wt78+wt88s;
%total degree of angle from t0 to t10
wt0=0;                      %starting point of angle (t0)
wt1=wt01;                   %starting point of angle (t0)to t1
wt2=wt12+wt1;               %starting point of angle (t0)to t2
wt3=wt23+wt2;               %starting point of angle (t0)to t3
wt4=wt34+wt3;               %starting point of angle (t0)to t4
wt4s=wt44s+wt4;             %starting point of angle (t0)to t5
wt5=wt4s5+wt4s;             %starting point of angle (t0)to t6
wt6=wt56+wt5;               %starting point of angle (t0)to t7
wt7=wt67+wt6;               %starting point of angle (t0)to t8
wt8=wt78+wt7;               %starting point of angle (t0)to t9
wt8s=wt88s+wt8;             %starting point of angle (t0)to t10
np_cycle=2080;
```

```
np01=10;
np12=1000;
np23=10;
np34=10;
np44s=10;
np4s5=10;
np56=1000;
np67=10;
np78=10;
np88s=10;
npoint=np_cycle*cycle;
n1=0;
inl=zeros(1,npoint);     %determine array for inl
vnc=zeros(1,npoint);     %determine array for vnc
time=zeros(1,npoint);
for(k1=1:cycle)           %create loop for number of cycle
% t0 to t1           %create loop for angle from t0 to t1
dwt01=wt01/np01;
for(k2=1:np01)
n1=n1+1;
time(n1)=(k1-1)*wts+(k2-1)*dwt01;
inl(n1)=-ino;                    %normalized inl
vnc(n1)=(-ino*dwt01*(k2-1))+1;    %normalized vnc
endfor
% t1 to t2          %create loop for angle from t1 to t2
dwt12=wt12/np12;
for(k2=1:np12)
n1=n1+1;
time(n1)=(k1-1)*wts+(k2-1)*dwt12+wt1;
inl(n1)=-ino*(sin(dwt12*(k2-1)+pi/2));    %normalized inl
vnc(n1)=0.5+(ino*cos(dwt12*(k2-1)+pi/2)); %normalized vnc
endfor
```

```
% t2 to t3          %create loop for angle from t2 to t3
dwt23=wt23/np23;
for(k2=1:np23)
n1=n1+1;
time(n1)=(k1-1)*wts+(k2-1)*dwt23+wt2;
inl(n1)=-sqrt(ino^2-0.5^2)+0.5*dwt23*(k2-1);
                                          %normalized inl
vnc(n1)=0;                                %normalized vnc
endfor
% t3 to t4           %create loop for angle from t3 to t4
dwt34=wt34/np34;
for(k2=1:np34)
n1=n1+1;
time(n1)=(k1-1)*wts+(k2-1)*dwt34+wt3;
inl(n1)=0.5*dwt34*(k2-1);                 %normalized inl
vnc(n1)=0;                                %normalized vnc
endfor
%t4 to t4s(dead time)%create loop for angle from t4 to t5
dwt44s=wt44s/np44s;
for(k2=1:np44s)
n1=n1+1;
time(n1)=(k1-1)*wts+(k2-1)*dwt44s+wt4;
inl(n1)=ino;                              %normalized inl
vnc(n1)=0;                                %normalized vnc
endfor
% t4s to t5         %create loop for angle from t5 to t6
dwt4s5=wt4s5/np4s5;
for(k2=1:np4s5)
n1=n1+1;
time(n1)=(k1-1)*wts+(k2-1)*dwt4s5+wt4s;
inl(n1)=ino;                              %normalized inl
vnc(n1)=ino*dwt4s5*(k2-1);                 %normalized vnc
```

```
endfor
% t5 to t6           %create loop for angle from t6 to t7
dwt56=wt56/np56;
for(k2=1:np56)
n1=n1+1;
time(n1)=(k1-1)*wts+(k2-1)*dwt56+wt5;
inl(n1)=ino*(sin(dwt56*(k2-1)+pi/2));     %normalized inl
vnc(n1)=0.5-(ino*cos(dwt56*(k2-1)+pi/2)); %normalized vnc
endfor
% t6 to t7           %create loop for angle from t7 to t8
dwt67=wt67/np67;
for(k2=1:np67)
n1=n1+1;
time(n1)=(k1-1)*wts+(k2-1)*dwt67+wt6;
inl(n1)=sqrt(ino^2-0.5^2)-0.5*(k2-1)*dwt67;%normalize inl
vnc(n1)=1;                                %normalized vnc
endfor
% t7 to t8           %create loop for angle from t8 to t9
dwt78=wt78/np78;
for(k2=1:np78)
n1=n1+1;
time(n1)=(k1-1)*wts+(k2-1)*dwt78+wt7;
inl(n1)=-0.5*dwt78*(k2-1);                %normalized inl
vnc(n1)=1;                                %normalized vnc
endfor
% t8 to t8s end of period (dead time)
dwt88s=wt88s/np88s; %create loop for angle from t9 to t10
for(k2=1:np88s)
n1=n1+1;
time(n1)=(k1-1)*wts+(k2-1)*dwt88s+wt8;
inl(n1)=-ino;                             %normalized inl
vnc(n1)=1;                                %normalized vnc
```

```
endfor
endfor
subplot(3,1,1);    %plot time on x axis and inl on y axis
plot(time,inl,'linewidth',3);
legend('inl');     %give name (inl) to graph
grid on;
subplot(3,1,2);    %plot time on x axis and vnc on y axis
plot(time,vnc,'linewidth',3);
legend('vnc');     %give name (vnc) to graph
grid on;
subplot(3,1,3);    %plot vnc on x axis and inl on y axis
plot(vnc,inl,'linewidth',3);
legend('vnc,inl'); %give name (vnc,inl) to graph
grid on;
```

Appendix B

The programming codes of the control characteristic of the proposed converter

```
%The programming codes of the control characteristic %of
the proposed converter

ino=[.6,1,2,4,8]; %determine ino=0.6, 1, 2, 4 and 8
min=100;
np=200;
m=zeros(1,np);
fns=zeros(1,np);
for(n0=1:5)
fnsmax=pi/((0.5/ino(n0))+asin(0.5/ino(n0))+(ino(n0)+sqrt(i
no(n0)^2-0.5^2))/0.5);
fnsmin=(pi/((0.5/ino(n0))+asin(0.5/ino(n0))+(ino(n0)+sqrt(
ino(n0)^2-0.5^2))/0.5))/min;
dnp=(fnsmax-fnsmin)/np;
for(n=1:np)
    fns(n)=(n-1)*dnp+fnsmin;
     m(n)=fns(n)/(pi)*(0.5*(pi/fns(n))-(0.125/ino(n0))-
(0.5*asin(0.5/ino(n0)))-ino(n0)-sqrt(ino(n0)^2-0.5^2));
 endfor
 plot(fns,m,'linewidth',3);%plot fns on x axis and m on y
axis
 hold on;
 endfor

grid on;
```

Appendix C

The programming codes of the range of $\omega_0 (t_2 - t_0)$ and $\omega_0 (t_3 - t_0)$ versus normalized load current (I_{no})

%The programming codes of the range of wo(t2-t0) and wo(t3-t0) versus normalized load current(ino)

```
inomin=0.5;          %determine minimum ino
inomax=2;            %determine maximum ino
vs=20;               %determine voltage source
io=2;                %determine load current
npoint=200;
tmax=inomax-inomin;
dt=tmax/npoint;
wot02=zeros(1,npoint);
wot03=zeros(1,npoint);
ino=zeros(1,npoint);
ino(1)=0.5;
wot02(1)=(0.5/ino(1))+asin(0.5/ino(1));
wot03(1)=wot02(1)+sqrt(ino(1)^2-0.25)/0.5;
for(n=2:npoint)
  ino(n)=ino(n-1)+dt;
  wot02(n)=(0.5/ino(n))+asin(0.5/ino(n));
  wot03(n)=wot02(n)+sqrt(ino(n)^2-0.25)/0.5;
endfor
plot(ino,wot02,'linewidth',3,ino,wot03,'linewidth',3);
grid on;
```

Biography

Name	Pornsak Techatanaset
Date of birth	26 December 1979
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